

# 1. PCIe/PXle-9516,9515 series Specifications

## Dynamic Signal Analyzer Module



📄 Please download [<JYPEDIA>](#), you can quickly check the product price and main features.

## Overview

The PXle-9516 series Dynamic Signal Analyzer is a powerful measurement instrument designed for the analysis of dynamic signals. With its high-resolution 24-bit ADC, it provides precise and accurate measurements for a wide range of applications. The simultaneous measurement capability of up to 16 channels allows for efficient analysis of multiple signals at once, saving time and effort. With a sampling rate of 256 kS/s, the instrument can capture signals with fine detail and fidelity. The voltage range options, ranging from  $\pm 0.3125$  V to  $\pm 10$  V, offer flexibility in accommodating different signal amplitudes. The dynamic range of 112 dB ensures the detection of both low and high-level signals, enabling comprehensive analysis. The inclusion of antialiasing filters prevents aliasing artifacts, ensuring accurate measurements. Additionally, the AC/DC coupling modes and provision of 4 mA IEPE make it compatible with a variety of sensors and signal sources. Overall, the PXle-9516 is a versatile and powerful tool for engineers and researchers involved in vibration analysis, acoustic measurements, and other dynamic signal analysis tasks.

## 1.1 Main Features

- 0.12% accuracy
- 24 bits resolution Synchronous acquisition
- 16 channels (JY-9516) / 8 channels (JY-9515) simultaneous measurement
- Sampling rate 256 kS/s
- Voltage Range :  $\pm 0.3125$  V,  $\pm 0.625$  V,  $\pm 1.25$  V,  $\pm 2.5$  V,  $\pm 5$  V,  $\pm 10$  V
- Dynamic Range : 112 dB
- Antialiasing filters
- Software-configurable AC/DC coupling per channel , 0.5 Hz cutoff frequency at AC couple
- Provide 4 mA IEPE for each channel
- Analog/Digital/Software trigger

## 1.2 Input Characteristic

Number of channels	16 (JY-9516) / 8 (JY-9515)
Input configuration	Pseudo-differential
Input coupling	AC/DC , selectable per channel
ADC resolution	24 bits
ADC type	Delta-sigma
Sample rate range	62.5 S/s-256 kS/s
Sample rate resolution	$\leq 0.0078125$ Sa/s
FIFO buffer size	512 MB
Data transfers	DMA
Positive terminal maximum working voltage	$\pm 12.5$ V
Negative terminal maximum working voltage	$\pm 1$ V
Positive terminal overvoltage protection (Voltages with respect to chassis ground)	$\pm 50$ V
Negative terminal overvoltage protection (Voltages with respect to chassis ground)	$\pm 1.7$ V
Input range	$\pm 0.3125$ V/ $\pm 0.625$ V/ $\pm 1.25$ V/ $\pm 2.5$ V/ $\pm 5$ V/ $\pm 10$ V
Input impedance (Between positive input and negative input)	10 M $\Omega$    35 pF
Input impedance (Between negative input and chassis ground)	50 $\Omega$
CMRR(Input frequency<20 kHz)	52 dB
IEPE Current	4 mA (software selectable, per channel)
IEPE Compliance	32 V
IEPE open	Software readable
IEPE short	Software readable
Channel input impedance with IEPE enabled (1 kHz)	>250 k $\Omega$
IEPE Current noise	100 pA/ $\sqrt{\text{Hz}}$

Table 1 Input Characteristic

## 1.3 Flatness

Flatness (51.2kS/s, for 1Hz - 20.48kHz input)	$\pm 0.003$ dB
Flatness (128kS/s, for 20.48kHz - 51.2kHz input)	$\pm 0.02$ dB
Flatness (256kS/s, for 51.2kHz - 102.4 kHz input)	$\pm 0.05$ dB

Table 2 Flatness

## 1.4 Dynamic Characteristics

Alias Rejection	108 dBc
-3dB Bandwidth	0.433 * Fs
-3 dB cutoff frequency in AC Couple mode	0.4 Hz
-0.1 dB cutoff frequency in AC Couple mode	4.5 Hz
Idle channel noise ( $\pm 10V$ , 51.2kS/s)	-94 dBVrms (20 $\mu$ Vrms)
Idle channel noise ( $\pm 0.3125V$ , 51.2kS/s)	-112 dBVrms (3 $\mu$ Vrms)
Idle channel noise ( $\pm 10V$ , 256kS/s)	-87 dBVrms (45 $\mu$ Vrms)
Idle channel noise ( $\pm 0.3125V$ , 256kS/s)	-105 dBVrms (6 $\mu$ Vrms)
Spectral noise density (at $\pm 0.3125V$ , around 1kHz)	20nVrms/VHz
Dynamic range( $\pm 10V$ 51.2kS/s)	112 dB
Dynamic range( $\pm 0.3125V$ 51.2kS/s)	101 dB
Dynamic range( $\pm 10V$ 256kS/s)	106 dB
Dynamic range( $\pm 0.3125V$ 256kS/s)	94 dB
Spurious free dynamic range (SFDR) ( $\pm 5V$ )*	105 dBc
Spurious free dynamic range (SFDR) ( $\pm 0.3125V$ )*	100 dBc
Total harmonic distortion plus noise (THD+N) ( $\pm 5V$ 51.2kS/s)*	-96 dBc
Total harmonic distortion plus noise (THD+N) ( $\pm 0.3125V$ 51.2kS/s)*	-84 dBc
Total harmonic distortion plus noise (THD+N) ( $\pm 5V$ 256kS/s)*	-95 dBc
Total harmonic distortion plus noise (THD+N) ( $\pm 0.3125V$ 256kS/s)*	-81 dBc
Crosstalk for adjacent ( $\pm 10V$ for 1kHz in)	-120 dBc
Crosstalk for adjacent ( $\pm 0.3125V$ for 1kHz in)	-110 dBc
Crosstalk for adjacent ( $\pm 10V$ for 102.4kHz in)	-92 dBc
Crosstalk for adjacent ( $\pm 0.3125V$ for 102.4kHz in)	-92 dBc
Filter Delay (Max, Normal Filter Mode)	37 Samples
Interchannel phase mismatch ( $\pm 10V$ for 20kHz in)	<0.17°
Interchannel phase mismatch ( $\pm 0.3125V$ for 20kHz in)	<0.30°
Interchannel phase mismatch ( $\pm 10V$ for 102.4kHz in)	<0.64°
Interchannel phase mismatch ( $\pm 0.3125V$ for 102.4 kHz in)	<1.35°

\*:Dynamic measurement indicators, including Total Harmonic Distortion plus Noise (THD+N) and Spurious-Free Dynamic Range (SFDR), are tested under the following conditions:

- Tone: 2kHz
- Amplitude: -1dBFS

Table 3 Dynamic Characteristics

Filter Delay in different mode and sample rate		
Sample Rate Range (Sa/s)	Filter Mode	
	Normal Mode	Wide BW Mode
[62.5,4000]	32.898	32.898
(4000, 32000]	35.875	35.875
(32000, 128000]	37	49
(128000,256000]	37	N/A

Table 4 Filter Delay

## 1.5 DC Couple Measurement Accuracy

<b>JY-9516 Basic Accuracy = <math>\pm(\% \text{ Reading} + \% \text{ Range})</math></b>								
Nominal Range (V)	24 Hour Tcal $\pm 1^\circ\text{C}$			90 Days Tcal $\pm 5^\circ$			24 Hr Full Scale Accuracy	90 Days Full Scale Accuracy
0.3125	0.06	+	0.33	0.10	+	0.31	1.2 mV	1.3 mV
0.625	0.04	+	0.16	0.08	+	0.16	1.2 mV	1.5 mV
1.25	0.06	+	0.08	0.10	+	0.08	1.7 mV	2.2 mV
2.5	0.06	+	0.04	0.11	+	0.04	2.5 mV	3.5 mV
5	0.09	+	0.03	0.10	+	0.03	5.4 mV	5.9 mV
10	0.09	+	0.02	0.10	+	0.02	9.4 mV	11.0 mV

Table 5 DC Basic Measurement Accuracy

<b>JY-9516 Additional Accuracy Adjustment = <math>\pm(\% \text{ Reading} + \% \text{ Range})</math></b>				
Nominal Range (V)	Temperature Coefficients ( $/^\circ\text{C}$ )			Full-Scale Temp Adjustment ( $\mu\text{V}/^\circ\text{C}$ )
0.3125	0.0011	+	0.0008	6 $\mu\text{V}$
0.625	0.0012	+	0.0006	11 $\mu\text{V}$
1.25	0.0011	+	0.0004	17 $\mu\text{V}$
2.5	0.0011	+	0.0003	33 $\mu\text{V}$
5	0.0011	+	0.0003	66 $\mu\text{V}$
10	0.0011	+	0.0002	130 $\mu\text{V}$

Table 6 DC Additional Measurement Accuracy

### 1.5.1 DC System Noise

Range (V)	SystemNoise( $\mu\text{Vrms}$ )
0.3125	5.7
0.625	6.3
1.25	8.1
2.5	14
5	25
10	47

Table 7 DC System Noise of JY-9516

## 1.6 AC Couple Measurement Accuracy

Gain error (Operating temperature within 5 °C of last self-calibration temperature):	0.05 dB
Offset error (Operating temperature within 5 °C of last self-calibration temperature):	±10 mV

Table 8 AC Couple Measurement Accuracy

## 1.7 Time Base

Accuracy	±0.3 ppm
Aging (first year @ + 25°C)	±1.0 ppm
Aging (20 year @ + 25°C)	±4.6 ppm

Table 9 Time Base

## 1.8 Bus Interface

Bus support	PXIe
Synchronization(PXIe)	CLK_100

Table 10 Bus Interface

## 1.9 Power Requirements

+3.3 V	3.0 A, maximum, maximum/warranted
+12 V	2.0 A, maximum, maximum/warranted

Table 11 Power Requirements

## 1.10 Triggers

Trigger Type	Analog / Digital / Software
Analog Trigger Voltage Range	Software Programmable
Trigger Mode	Start / Reference / ReTrigger
Digital Trigger Source	Ext Trigger Pin
Digital Trigger Compatibility	5 V TTL
Interval of ReTrigger	5 Samples

Table 12 Triggers

## 1.11 Physical

Dimensions	Standard 3U PXI
Weight	0.23 kg

Table 13 Physical

## 1.12 Environment specification

Operating environment	0-55 °C
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Table 14 Environment specification

## 1.13 Connector

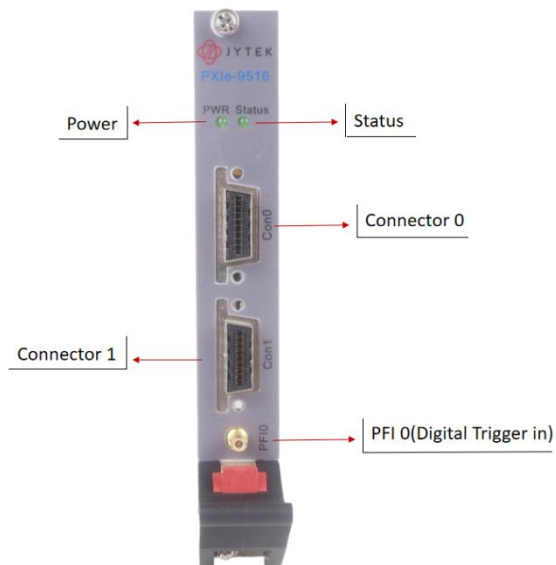


Figure 1 PXIe-9516 Front Panel

## 1.14 Pin Definition

Signal Name	Con0	Signal Name	Cable	Pin Notes	
	G1	GND1		G1,G2,G3,G4,G5,G6,G7,G8,G9	GND*
AI7-	S2   S1	AI7+	CH7	S1	AI7+
	G2	GND2		S2	AI7-
AI6-	S4   S3	AI6+	CH6	S3	AI6+
	G3	GND3		S4	AI6-
AI5-	S6   S5	AI5+	CH5	S5	AI5+
	G4	GND4		S6	AI5-
AI4-	S8   S7	AI4+	CH4	S7	AI4+
	G5	GND5		S8	AI4-
AI3-	S10   S9	AI3+	CH3	S9	AI3+
	G6	GND6		S10	AI3-
AI2-	S12   S11	AI2+	CH2	S11	AI2+
	G7	GND7		S12	AI2-
AI1-	S14   S13	AI1+	CH1	S13	AI1+
	G8	GND8		S14	AI1-
AI0-	S16   S15	AI0+	CH0	S15	AI0+
	G9	GND9		S16	AI0-
				*All GND signal lines are connected together	

Table 15 Connector 0



signal	Con1	signal	Cable	Pin Notes	
	G1	GND1		G1,G2,G3,G4,G5,G6,G7,G8,G9	GND*
AI15-	S2   S1	AI15+	CH15	S1	AI15+
	G2	GND2		S2	AI15-
AI14-	S4   S3	AI14+	CH14	S3	AI14+
	G3	GND3		S4	AI14-
AI13-	S6   S5	AI13+	CH13	S5	AI13+
	G4	GND4		S6	AI13-
AI12-	S8   S7	AI12+	CH12	S7	AI12+
	G5	GND5		S8	AI12-
AI11-	S10   S9	AI11+	CH11	S9	AI11+
	G6	GND6		S10	AI11-
AI10-	S12   S11	AI10+	CH10	S11	AI10+
	G7	GND7		S12	AI10-
AI9-	S14   S13	AI9+	CH9	S13	AI9+
	G8	GND8		S14	AI9-
AI8-	S16   S15	AI8+	CH8	S15	AI8+
	G9	GND9		S16	AI8-
				*All GND signal lines are connected together	

Table 16 Connector 1

## 1.15 Physical and Environment

Dimensions:	3 U CompactPCI slot
Weight:	220 g

Table 17 Physical Specification

Operating environment:	0-55 °C
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Table 18 Environment Specification

## 1.16 Special Operating Restriction

**The amplitude of the out-of-band signal between 0.3M and 3MHz must be less than 20% of full scale.<sup>1</sup>**

1. This restriction does not affect applications where PXle-9516 is connected to the front-end sensors such as microphones and accelerators because these sensors have built-in attenuation so that the out-of-band voltage will not exceed 20% of full scale. If you have question on this restriction, please contact JYTEK for more information.

### 1.17 Optimizing Precision: Custom Gain Error Calibration for Fixed Sampling Rates

The gain error of the 9516 model varies with different sampling rates, and the specifications provided in this manual cover the error range across all potential sampling rates.

If users calibrate the gain error of their acquisition card for their specific sampling rate, they can achieve an accuracy that surpasses the general specifications that encompass all sampling rates.

### 1.18 Synchronization Accuracy

	9516/9516T
Synchronization Accuracy (Single module)	30ns
Synchronization Accuracy (Two modules in one chassis)	30ns

Table 19 Synchroniazation Accuracy

## 2. Order Information

- PXIe-9516 (PN: JY1951601-01)  
16-CH 24-Bit 256 kS/s PXIe High-Resolution Dynamic Signal Acquisition Module
- PXIe-9515 (PN: JY4808423-01)  
8-CH 24-Bit 256 kS/s PXIe High-Resolution Dynamic Signal Acquisition Module
- PCIe-9516 (PN: JY1136217-01)  
16-CH 24-Bit 256 kS/s PCIe High-Resolution Dynamic Signal Acquisition Module
- PCIe-9515 (PN: JY9236872-01)  
8-CH 24-Bit 256 kS/s PCIe High-Resolution Dynamic Signal Acquisition Module
- Accessory  
ACL-2000802-02 (PN: JY2000802-02)  
20 cm, 8-CH shielded x4 InfiniBand to BNC cable

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Specs and Manual Version: V1.0.4

Revision Date: September 11, 2025

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signal	Con1		signal	Cable	Pin Notes	
	G1		GND1		G1,G2,G3,G4,G5,G6,G7,G8,G9	GND*
AI15-	S2	S1	AI15+	CH15	S1	AI15+
	G2		GND2		S2	AI15-
AI14-	S4	S3	AI14+	CH14	S3	AI14+
	G3		GND3		S4	AI14-
AI13-	S6	S5	AI13+	CH13	S5	AI13+
	G4		GND4		S6	AI13-
AI12-	S8	S7	AI12+	CH12	S7	AI12+
	G5		GND5		S8	AI12-
AI11-	S10	S9	AI11+	CH11	S9	AI11+
	G6		GND6		S10	AI11-
AI10-	S12	S11	AI10+	CH10	S11	AI10+
	G7		GND7		S12	AI10-
AI9-	S14	S13	AI9+	CH9	S13	AI9+
	G8		GND8		S14	AI9-
AI8-	S16	S15	AI8+	CH8	S15	AI8+
	G9		GND9		S16	AI8-
					*All GND signal lines are connected together	

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## 4. Software

### 4.1 System Requirements

JY-9516 boards can be used in a Windows or a Linux operating system.

Microsoft Windows: Windows 7 32/64 bit, Windows 10 32/64 bit.

Linux Kernel Versions: There are many Linux versions. It is not possible JYTEK can support and test our devices under all different Linux versions. JYTEK will at the best support the following Linux versions.

Linux Version
Ubuntu LTS
16.04: 4.4.0-21-generic(desktop/server)
16.04.6: 4.15.0-45-generic(desktop) 4.4.0-142-generic(server)
18.04: 4.15.0-20-generic(desktop) 4.15.0-91-generic(server)
18.04.4: 5.3.0-28-generic (desktop) 4.15.0-91-generic(server)
Localized Chinese Version
中标麒麟桌面操作系统软件（兆芯版）V7.0（Build61）: 3.10.0-862.9.1.nd7.zx.18.x86_64
中标麒麟高级服务器操作系统软件V7.0U6: 3.10.0-957.el7.x86_64

Table 20 Supported Linux Versions

### 4.2 System Software

When using the JY-9516 in the Window environment, you need to install the following software from Microsoft website:

Microsoft Visual Studio Version 2015 or above,

.NET Framework version is 4.0 or above.

.NET Framework is coming with Windows 10. For Windows 7, please check .NET Framework version and upgrade to 4.0 or later version.

Given the resources limitation, JYTEK only tested JY-9516 be with .NET Framework 4.0 with Microsoft Visual Studio 2015. JYTEK relies on Microsoft to maintain the compatibility for the newer versions.

### 4.3 C# Programming Language

All JYTEK default programming language is Microsoft C#. This is Microsoft recommended programming language in Microsoft Visual Studio and is particularly suitable for the test and measurement applications. C# is also a cross platform programming language.

### 4.4 JY-9516 Series Hardware Driver

After installing the required application development environment as described above, you need to install the JY-9516 hardware driver.

JYTEK hardware driver has two parts: the shared common driver kernel software (FirmDrive) and the specific hardware driver.

**Common Driver Kernel Software (FirmDrive):** FirmDrive is the JYTEK's kernel software for all hardware products of JYTEK instruments. You need to install the FirmDrive software before using any other JYTEK hardware products. FirmDrive only needs to be installed once. After that, you can install the specific hardware driver.

**Specific Hardware Driver:** Each JYTEK hardware has a C# specific hardware driver. This driver provides rich and easy-to-use C# interfaces for users to operate various JY-9516 function. JYTEK has standardized the ways which JYTEK and other vendor's DSA modules are used by providing a consistent user interface, using the methods, properties and enumerations in the object-oriented programming environment. Once you get yourself familiar with how one JYTEK DAQ card works, you should be able to know how to use all other DAQ hardware by using the same methods.

**Note that this driver does not support cross-process, and if you are using more than one function, it is best to operate in one process.**

### 4.5 Install the SeeSharpTools from JYTEK

To efficiently and effectively use JY-9516 boards, you need to install a set of free C# utilities, SeeSharpTools from JYTEK. The SeeSharpTools offers rich user interface functions you will find convenient in developing your applications. They are also needed to run the examples come with JY-9516 hardware. Please register and download the latest SeeSharpTools from our website, [www.jytek.com](http://www.jytek.com).



## 4.6 Running C# Programs in Linux

Most C# written programs in Windows can be run by MonoDevelop development system in a Linux environment. You would develop your C# applications in Windows using Microsoft Visual Studio. Once it is done, run this application in the MonoDevelop environment. This is JYTEK recommended way to run your C# programs in a Linux environment.

If you want to use your own Linux development system other than MonoDevelop, you can do it by using our Linux driver. However, JYTEK does not have the capability to support the Linux applications. JYTEK completely relies upon Microsoft to maintain the cross-platform compatibility between Windows and Linux using MonoDevelop.

## 5. JYPEDIA

JYPEDIA is an excel file. It contains JYTEK product information, pricing, inventory information, drivers, software, technical support, knowledge base etc. You can register and download a [JYPEDIA](http://www.jytek.com) excel file from our web [www.jytek.com](http://www.jytek.com). JYTEK highly recommends you use this file to obtain information from JYTEK.

## 6. Operation JY-9516/9515

### 6.1 Quick Start

After you have installed the driver software and the SeeSharpTools, you are ready to use Microsoft Visual Studio C# to operate the JY-9516/JY-9515 products. The JY-9515 and JY-9516 have no operational differences. The only difference is the number of sampling channels. This chapter will take JY-9516 as an example for the introduction. If you are already familiar with Microsoft Visual Studio C#, the quickest way to use JY-9516 boards is to go through our extensive examples. We provide source code of our examples. In many cases, you can modify the source code and start to write your applications. We also provide Learn by Example in the following sections. These examples will help you navigate and learn how to use this JY-9516.

### 6.2 Acquisition Methods

JY-9516 uses a  $\Delta\Sigma$  modulator and a digital filter to acquire analog signals, which can realize the acquisition of 16 channels of analog signals. You need to configure AI channels and set up some parameters through JY-9516 driver software. The most

important parameters are Data Acquisition mode, Sample Rate, SamplesToAcquire, Channel Count, Channel Range, Coupling mode (DC/AC) and IEPE. For Data Acquisition, JY-9516 provides 3 acquisition modes: Continuous, Finite and Single Point.

**SampleRate:** How fast data are acquired per second per channel. For example, if the sample rate is 1000Hz, you acquire two channels of data, you will have 2000 points/second.

**SamplesToAcquire:** This parameter behaves differently in the different AI acquisition modes. In the continuous acquisition mode, SamplesToAcquire is the buffer size used JY-9516 in the AI acquisition task, please see Section 6.2.1; in the finite acquisition mode, it is the total number of samples to capture, please see Section 6.2.2.

**Channel Count:** how many channels you want to collect data. You can select the channels required for this acquisition. JY-9516 simultaneously collects data from the channels.

**Coupling mode:** The coupling method of JY-9516 with the signal is as follows. In DC coupling mode, JY-9516 is directly connected to the signal under test. In AC mode, JY-9516 is connected to the signal under test through a coupling capacitor, which removes the DC component from the signal.

**IEPE:** Each channel of JY-9516 can provide 4mA IEPE, making it compatible with a variety of sensors and signal sources. It is recommended to use the AC coupling mode when IEPE is enabled.

## Learn by example 6.2.

- Connect the signal source to JY-9516 AI0 Channel and AI1 Channel using BNC cables, Set two sine wave signal ( $f = 1K$ ,  $V_{pp} = 10V$ ;  $f=3K$   $V_{pp} = 5V$ ).
- Open **Winform AI Continuous Multi-Channel**, Click Enable/Disable all combobox, Select CH0 and CH1, use default range set and Coupling set, do not enable IEPE. This example program will continuously acquire from multiple channels.
- SampleRate is set by **Sample Rate**
- **Samples to Acquire** is the samples to be acquired for each channel in one block. The continuous mode will acquire blocks after blocks until Stop button is pressed.
- When start is clicked, it generates a software trigger, which starts the acquisition.
- The result is shown below.

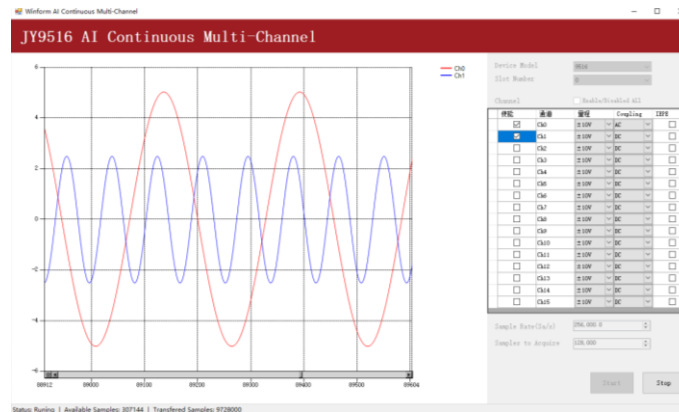


Figure 2 Acquisition Result

## 6.2.1 Continuous Acquisition

An AI acquisition task will acquire the data continuously until the task is stopped. The JY-9516 device will continue acquiring data and save the data in a FIFO buffer. You specify how many samples to read back by the user buffer's length, if your program does not read the data fast enough, the FIFO buffer may overflow. In this case, the driver software will throw out an error message.

## 6.2.2 Finite Acquisition

In the Finite Acquisition mode, an AI acquisition task will capture specific total number of samples by the parameter, SamplesToAcquire. You can use the sample program **Winform AI Finite** to learn more about Finite Acquisition.

## 6.2.3 Single Point

Acquisition In the Single Acquisition mode, it is to capture a single sample for each acquisition. You can use sample program: **Console AI Single Point** to learn more about the single point acquisitions

## 6.3 Trigger Source

JY-9516 has 4 trigger types: Immediate trigger, Software trigger, Analog trigger, and Digital trigger. The trigger type is a property and set by driver software. Users can employ different triggering types to meet the measurement requirements under different working conditions

### 6.3.1 Immediate trigger

This trigger mode does not require configuration and is triggered immediately when an operation starts.

### Learn by example 6.3.1

Use the same program and connection as in **Learn by Example 6.2.**

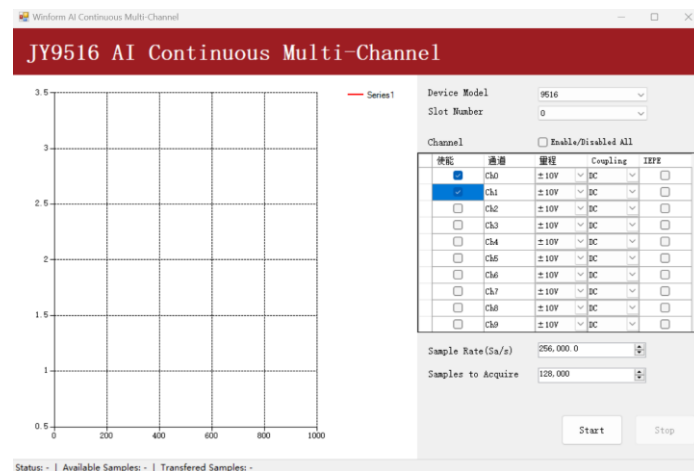


Figure 3 Parameter of Immediate trigger

With Immediate trigger you can click **Start** button to generate the task instead of sending a trigger signal.

### 6.3.2 Soft trigger

A software trigger must be configured by the driver software. The trigger starts when a trigger software routine is called.

### Learn by example 6.3.2

- Connect the signal source to JY-9516 AI0 Channel using BNC cable.
  - Set sine wave signal ( $f = 1K$ ,  $V_{pp} = 10V$ ).
  - Open **Winform AI Continuous Soft Trigger.**, Click Enable/Disable all combobox, Select CH0, use default range set and Coupling set, do not enable IEPE.
  - Click Start to run the task.
- Data will not be acquired until there is a positive signal from Software Trigger when Send Soft Trigger is clicked.
- After sending the trigger signal, the result will be shown in figure below:

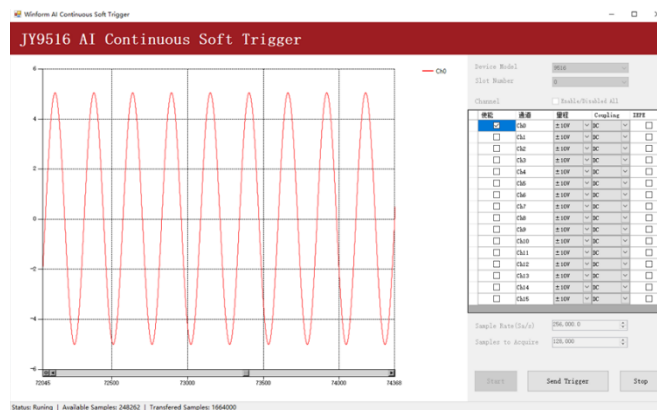


Figure 4 Acquisition result of soft trigger

### 6.3.3 External Analog Trigger

You can assign one of measurement channels as the analog trigger source. JY-9516 provides three analog trigger modes

- Edge comparator,
- Hysteresis comparator,
- Window comparator.

Analog trigger threshold range can be arbitrarily selected in the effective range of the selected channel. When setting the threshold, please pay attention to the physical unit currently in use.

#### Edge comparator

In the Edge comparator, there are two trigger conditions: *Rising Slope Trigger* and *Falling Slope Trigger*.

*Rising Slope Trigger*: The Edge comparator output is high when the signal goes above the threshold; the output is low when the signal goes below the threshold as shown in Figure 5 Rising Slope Trigger.

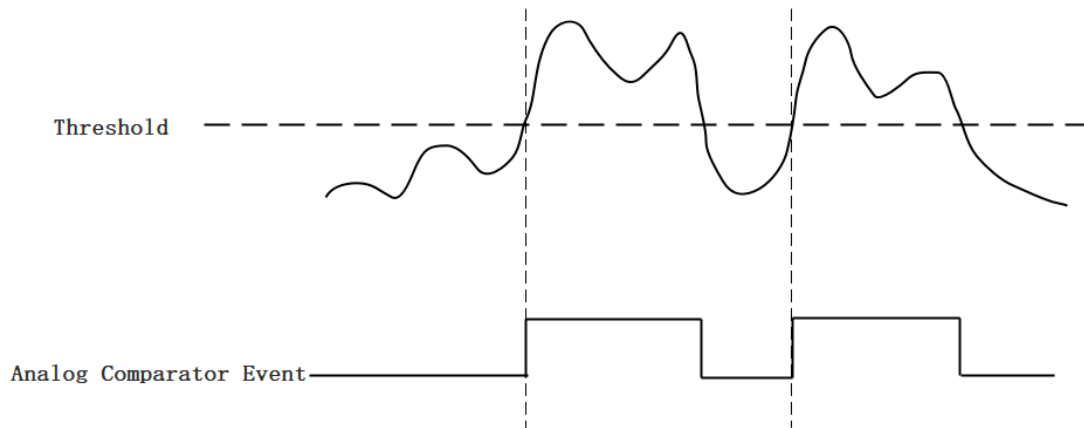


Figure 5 Rising Slope Trigger

**Falling Slope Trigger:** The Edge comparator output is high when the signal goes below the threshold; the output is low when the signal goes above the threshold as shown in Figure 6.

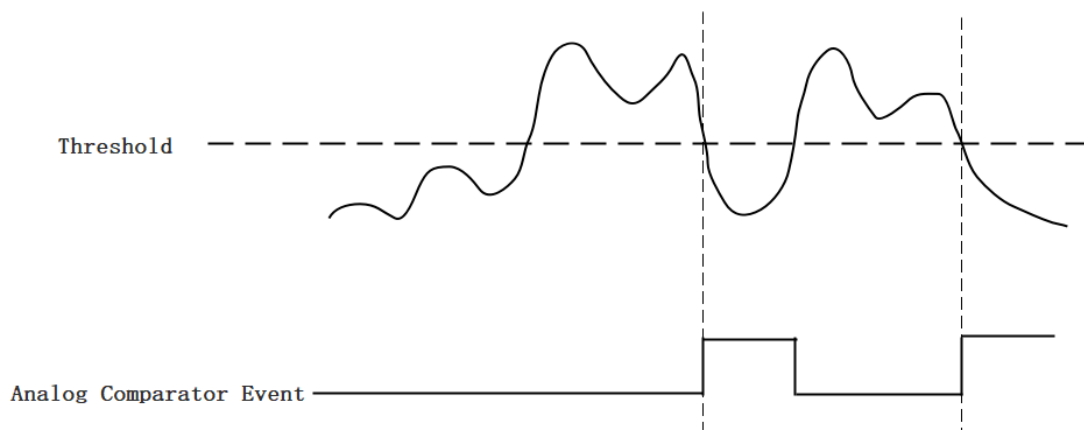


Figure 6 Falling Slope Trigger

## Hysteresis Comparator

The hysteresis comparator is designed for preventing spurious triggering. You can set hysteresis region by setting high threshold and low threshold. There are two trigger conditions: *Hysteresis with Rising Slope Trigger* and *Hysteresis with Falling Slope Trigger*.

**Hysteresis with Rising Slope Trigger:** The Hysteresis comparator output is high when the signal must first be below the low threshold, then goes above the high threshold. The output will change to low when the signal goes below the low threshold as shown in Figure 7.

**Hysteresis with Falling Slope Trigger:** The Hysteresis comparator output is high when the signal must first be above the high threshold, then goes below the low threshold. The output will change to low when the signal goes above the high threshold as shown in Figure 8.

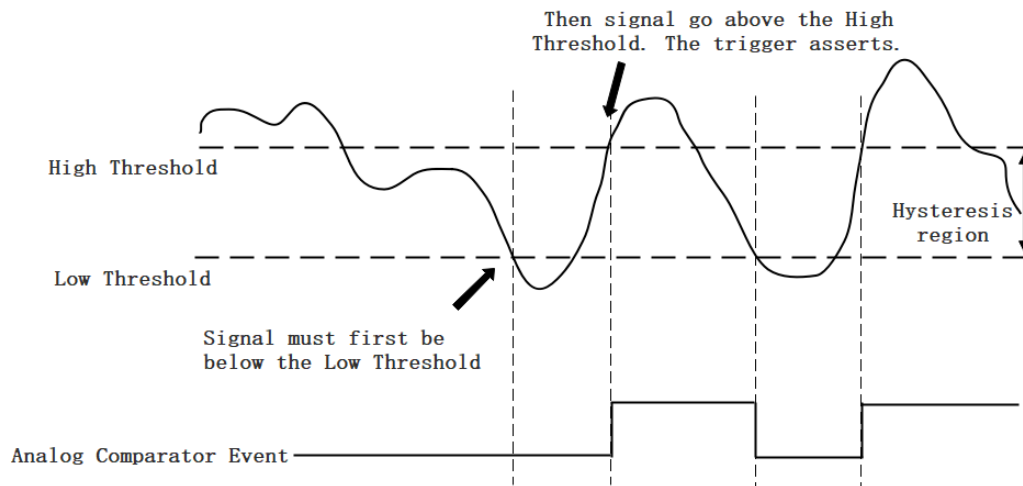


Figure 7 Hysteresis with Rising Slope Trigger

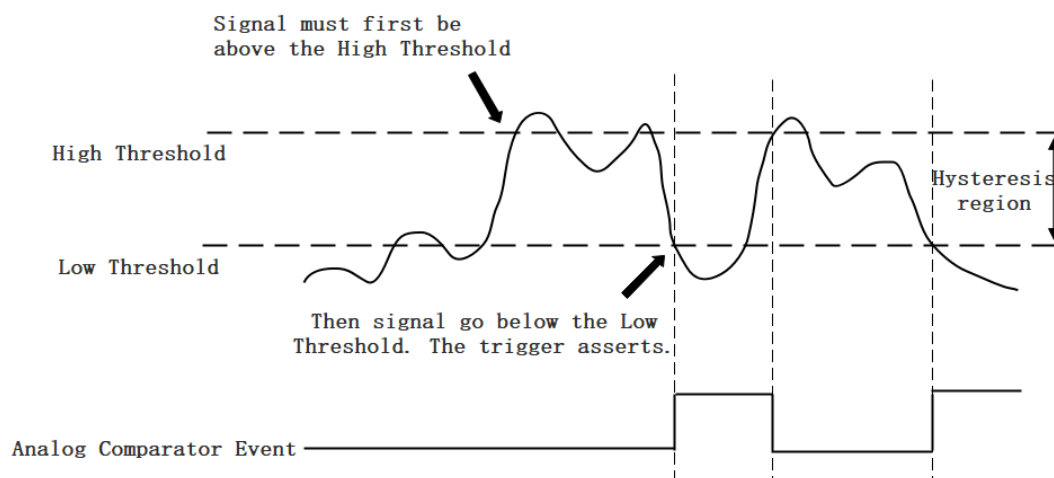


Figure 8 Hysteresis with Falling Slope Trigger

## Window comparator

The window comparator is designed to acquire signal from interesting window by setting High Threshold and Low Threshold. There are two trigger conditions: *Entering Window Trigger* and *Leaving Window Trigger*.

**Entering Window Trigger:** The window comparator output is high when the signal enters the window defined by the *Low Threshold* and *High Threshold*. The output will change to low when the signal leaves the window as shown in Figure 9.

**Leaving Window Trigger:** The window comparator output is high when the signal leaves the window defined by the *Low Threshold* and *High Threshold*. The output will change to low when the signal enters the window as shown in Figure 10.

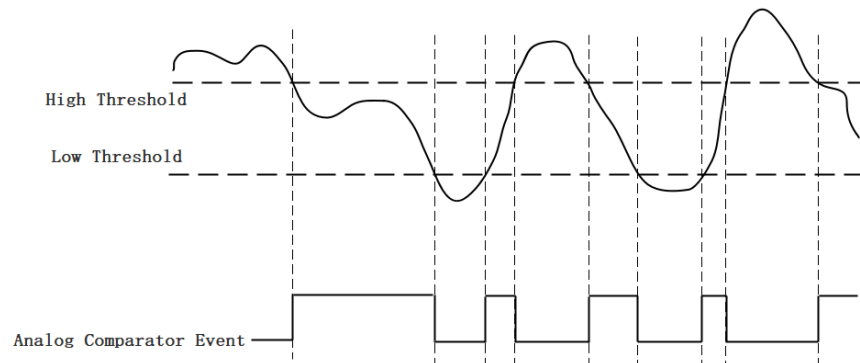


Figure 9 Entering Window Trigger

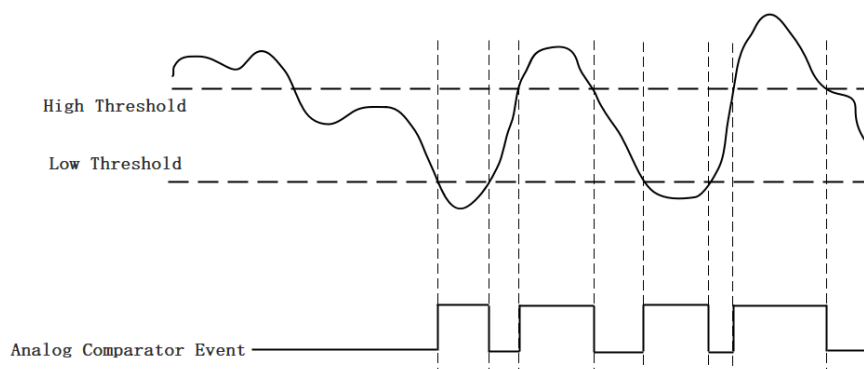


Figure 10 Leaving Window Trigger

### Learn by example 6.3.2

- Connect the signal source to JY-9516 AI0 Channel using BNC cable.
- Set sine wave signal ( $f = 1K$ ,  $V_{pp} = 10V$ ).
- Open **Winform AI Finite Analog Trigger**, set the following numbers as shown.



Device Model: 9616  
Slot Number: 0  
Channel: ☐ Enable/Disable All

使能	通道	量程	耦合	阻抗
<input checked="" type="checkbox"/>	Ch0	±10V	DC	<input type="checkbox"/>
<input type="checkbox"/>	Ch1	±10V	DC	<input type="checkbox"/>
<input type="checkbox"/>	Ch2	±10V	DC	<input type="checkbox"/>
<input type="checkbox"/>	Ch3	±10V	DC	<input type="checkbox"/>
<input type="checkbox"/>	Ch4	±10V	DC	<input type="checkbox"/>
<input type="checkbox"/>	Ch5	±10V	DC	<input type="checkbox"/>
<input type="checkbox"/>	Ch6	±10V	DC	<input type="checkbox"/>
<input type="checkbox"/>	Ch7	±10V	DC	<input type="checkbox"/>
<input type="checkbox"/>	Ch8	±10V	DC	<input type="checkbox"/>
<input type="checkbox"/>	Ch9	±10V	DC	<input type="checkbox"/>
<input type="checkbox"/>	Ch10	±10V	DC	<input type="checkbox"/>
<input type="checkbox"/>	Ch11	±10V	DC	<input type="checkbox"/>

Sample Rate(Sa/s): 256,000.0  
Samples to Acquire: 128,000  
Trg Mode: Start  
Pre Trigger Sample: 1024  
Retrigger Count: 0  
Anlg Trg Comparator: Edge  
Anlg Trg Edge: Rising  
Anlg Trg Src: Channel\_0  
Threshold: 2.0000  
-: -15.0000

Start Stop

Figure 11 Parameter of External Analog Trigger

- Modes of the *Analog Trigger* are set by **Anlg Trg Comparator**. Set it to **Edge**.
- The edge of *EdgeComparator* set by **Anlg Trg Edge**. (**Rising** and **Falling**). Set it to **Rising**.
- **Trigger source** can be any channel of JY-9516 analog input. Set it to **Channel\_0**.
- According to the rules of Rising mentioned above, the signal acquisition will not start until it raises to 2.0 V, which is set by **Threshold** above.
- Click Start to run the task.
- This indicates the data acquisition will start only after a triggering event. In this example a trigger signal will occur when the hysteresis comparator meets the condition.
- The result is shown below:

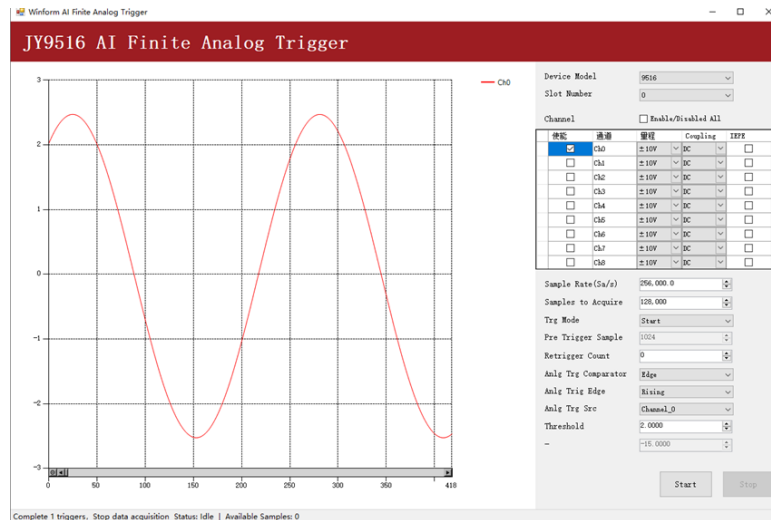


Figure 12 Acquisition result of Analog Trigger

### 6.3.4 External Digital Trigger

JY-9516 supports different external digital trigger sources from PXI Trigger bus (PXI\_TRIG<0..7>), PXI\_STAR and connectors of front panel (PFI0). The high pulse width of digital trigger signal must be longer than 20 ns for effective trigger. The module will monitor the signal on digital trigger source and wait for the rising edge or falling edge of digital signal which depending on the set trigger condition, then cause the module to acquire the data as shown in Figure 13.

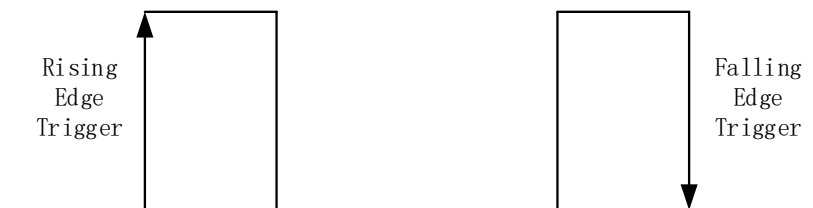


Figure 13 External Digital Trigger

#### Learn by Example 6.3.4

- Connect the signal source to JY-9516 AI0 Channel and PFI0 Channel using BNC cables.
- Set sine wave signal ( $f=1K$ ,  $V_{pp}=5V$ ) for AI0 Channel and square wave signal ( $f=1k$ ,  $V_{pp}=5V$ , Duty = 5%) for PFI0 Channel.
- Open **Winform AI Finite Digital Trigger**, set the following numbers as shown

below.

使能	通道	量程	Coupling	IEPE
<input checked="" type="checkbox"/>	Ch0	±10V	DC	<input type="checkbox"/>
<input type="checkbox"/>	Ch1	±10V	DC	<input type="checkbox"/>
<input type="checkbox"/>	Ch2	±10V	DC	<input type="checkbox"/>
<input type="checkbox"/>	Ch3	±10V	DC	<input type="checkbox"/>
<input type="checkbox"/>	Ch4	±10V	DC	<input type="checkbox"/>
<input type="checkbox"/>	Ch5	±10V	DC	<input type="checkbox"/>
<input type="checkbox"/>	Ch6	±10V	DC	<input type="checkbox"/>
<input type="checkbox"/>	Ch7	±10V	DC	<input type="checkbox"/>
<input type="checkbox"/>	Ch8	±10V	DC	<input type="checkbox"/>

Figure 14 Parameter of Digital Trigger

- *Trigger Source* is set by **Dgt Trg Src**, set it to **Ext\_Trig**.
- There are two **Trigger Edge**: **Rising** and **Falling**, set it to **Rising**.
- Click **Start** and the result shows below:

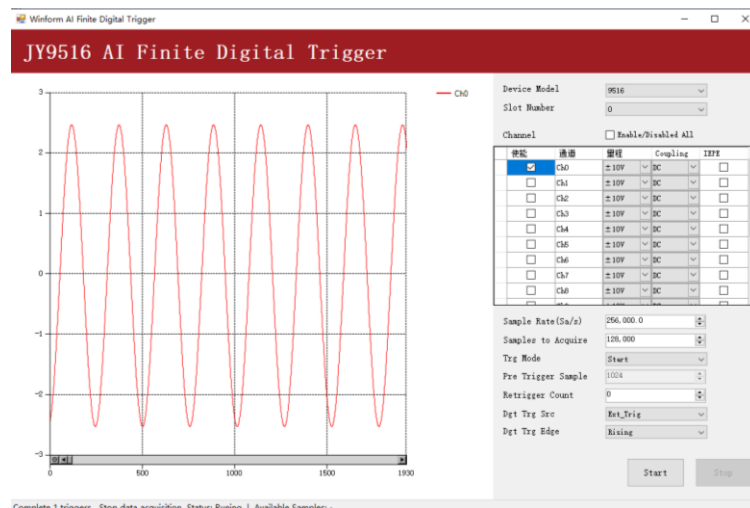


Figure 15 Digital Trigger Acquisition

- Since the squarewave is used for the digital trigger source, when a rising edge of the squarewave occurs, the digital trigger will be activated, and the data acquisition will start.

## 6.4 Trigger Mode

The JY-9516's analog inputs support several trigger modes: start trigger, reference trigger, and re-trigger.

### 6.4.1 Start Trigger

In this mode, data acquisition begins immediately after the trigger. This trigger mode is suitable for continuous acquisition and finite acquisition. As shown in Figure 16.

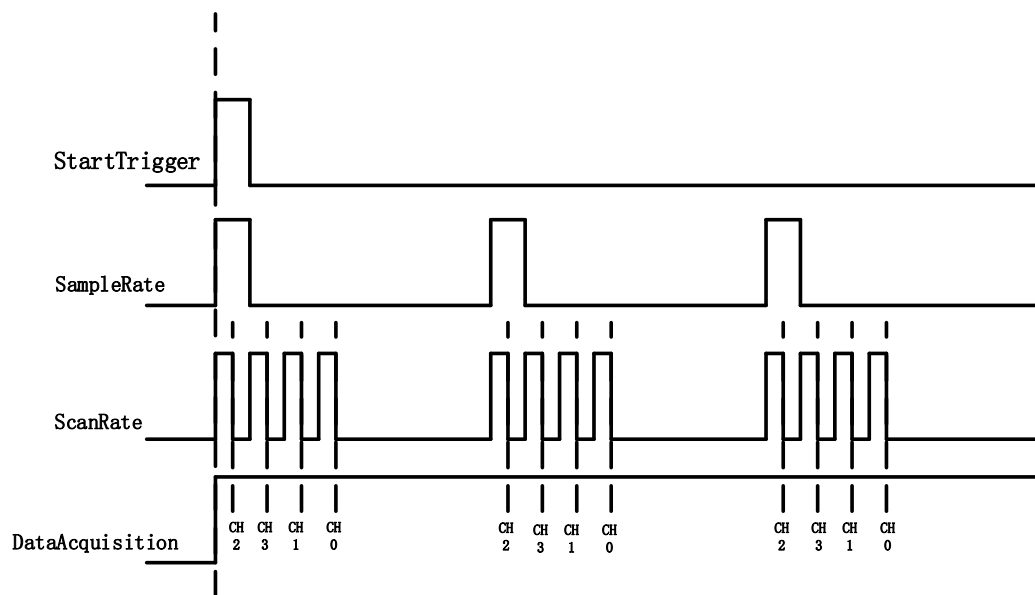


Figure 16 Start Trigger

### 6.4.2 Reference Trigger

This trigger mode is suitable for finite acquisition. In this mode, user can set the number of pre-trigger samples. The default number of pre-trigger points is 0. First you need to start the data acquisition. When the reference trigger condition is met, the routine will return the acquired data points. If when the points less than the pre-trigger samples, the trigger signal be ignored. An example is show below.

Example

- Total samples: 1000;
- Channel Count: 1
- Pre-trigger samples: 10;

- After triggering, it returns total 1000 samples, 10 being pre-triggered, 990 after triggering

The principle is shown in Figure 17.

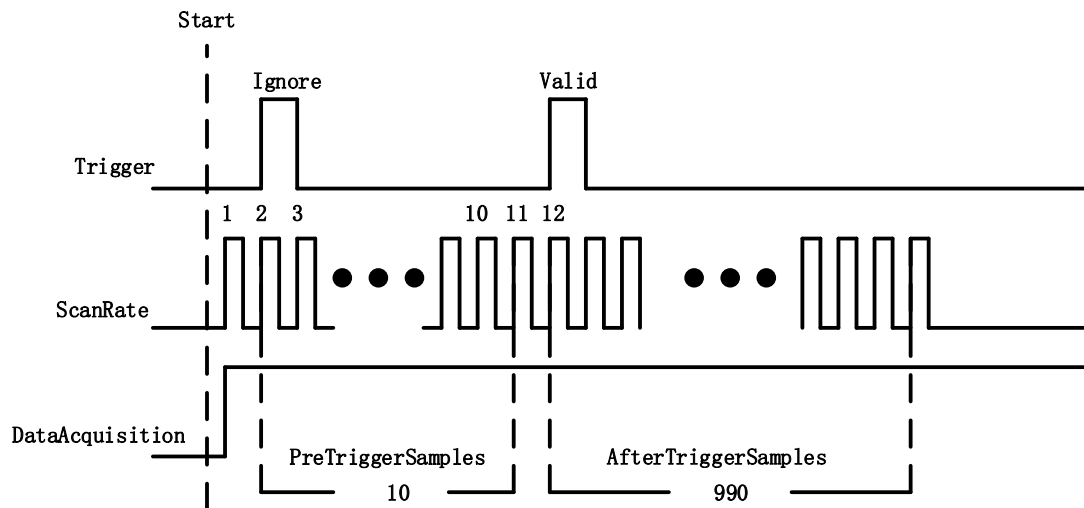


Figure 17 Reference Trigger

### 6.4.3 ReTrigger

JY-9516 series products support retrigger mode. In the retrigger mode, you can set the number of retrigger and the length of each acquisition. Assuming that the number of re triggers is  $n$  and the length of each trigger acquisition is  $m$ , the length of all acquisition data is  $n * m * \text{channel count}$ . Show in Figure 18.

When the number of retriggers is - 1, it is infinite.

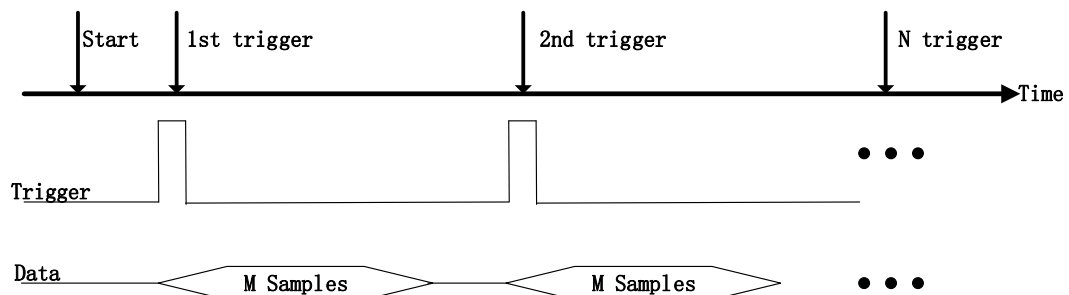


Figure 18 ReTrigger

## Learn by Example 6.4

- Connect the signal source to JY-9516 AI0 Channel using BNC cable.
- Set sine wave signal ( $f = 1K$ ,  $V_{pp} = 5V$ ).
- Open **Winform AI Finite Analog Trigger**, set the following numbers as shown.

Device Model: 9516  
Slot Number: 0  
Channel: ☐ Enable/Disabled All

使能	通道	量程	Coupling	IEPE
<input checked="" type="checkbox"/>	Ch0	±10V	DC	<input type="checkbox"/>
<input type="checkbox"/>	Ch1	±10V	DC	<input type="checkbox"/>
<input type="checkbox"/>	Ch2	±10V	DC	<input type="checkbox"/>
<input type="checkbox"/>	Ch3	±10V	DC	<input type="checkbox"/>
<input type="checkbox"/>	Ch4	±10V	DC	<input type="checkbox"/>
<input type="checkbox"/>	Ch5	±10V	DC	<input type="checkbox"/>
<input type="checkbox"/>	Ch6	±10V	DC	<input type="checkbox"/>
<input type="checkbox"/>	Ch7	±10V	DC	<input type="checkbox"/>
<input type="checkbox"/>	Ch8	±10V	DC	<input type="checkbox"/>
<input type="checkbox"/>	Ch9	±10V	DC	<input type="checkbox"/>
<input type="checkbox"/>	Ch10	±10V	DC	<input type="checkbox"/>
<input type="checkbox"/>	Ch11	±10V	DC	<input type="checkbox"/>

Sample Rate(Sa/s): 256,000.0  
Samples to Acquire: 128,000  
Trg Mode: Start  
Pre Trigger Sample: 1000  
Retrigger Count: 0  
Anlg Trg Comparator: Edge  
Anlg Trg Edge: Rising  
Anlg Trg Src: Channel\_0  
Threshold: 2.0000  
-: -15.0000

Start Stop

Figure 19 Parameter setting of Start Trigger Mode

- You can use three different kinds of triggers in this program as mentioned in **6.4**. *Start Trigger* and *Reference Trigger* can be set by **Trigger Mode**. For *ReTrigger* can be used by changing the numbers in **Retrigger Count**.
- *PretriggerSamples* is set by **Pretrigger Samples**.
- Now the trigger is a **Start Trigger**. Click **Start** to begin the data acquisition, the result is shown below:

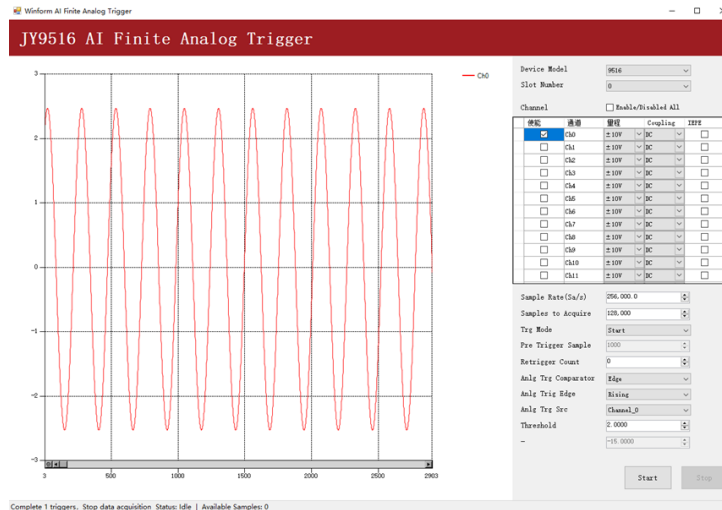


Figure 20 Retrigger in Start Trigger Mode

- Now change the **Trigger Mode** to **Reference** mode with **Pretrigger Samples** 1000. A different result shows below:

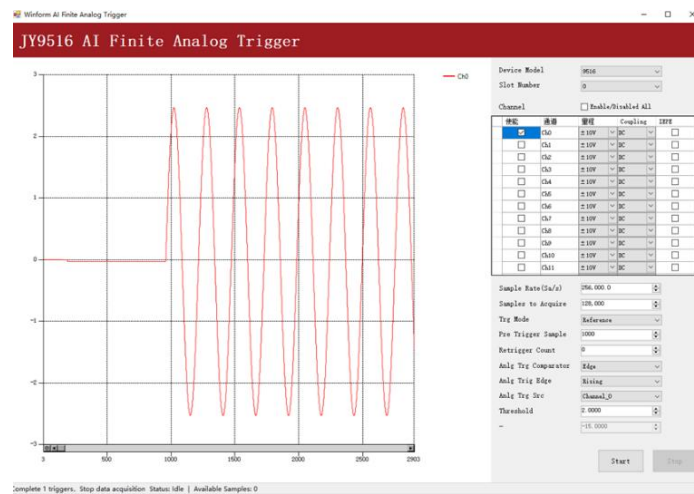


Figure 21 Acquisition of Reference mode

- You can see the horizontal movement between two signals due to the change of **Trigger Mode**.

## 6.5 Sync

When executing multi-channel acquisition, all channels of the single JY-9516 are acquired synchronously.

When two or more JY-9516 cards are working simultaneously, it is necessary to synchronize the clocks of the multiple JY-9516 cards in advance to ensure the synchronicity of signal acquisition.

The JY-9516 cards waiting for synchronization are divided into a master card and slave cards. Only one master card is allowed at the same time, which will provide the sampling clock. All slave cards will measure based on the clock signal provided by the master card.

### Learn by Example 6.5

- Connect the same signal source to JY-9516(PXle chassis Slot 2) AIO Channel and JY-9516(PXle chassis Slot3) AIO Channel using BNC cables. The BNC cables are in parallel.
- Set sine wave signal ( $f=1K$ ,  $V_{pp}=5V$ ).
- Open **Winform AI Multi-Device Sync**, set the following numbers as shown.

Device Model	9516
Slot Number (Master)	2
Slot Number (Slave)	3
<b>Acquire</b>	
Channel (Master)	Ch0
Channel (Slave)	Ch0
Sample Rate(Sa/s)	256,000.0
Samples to Acquire	128,000
Reference Clock	PXI_Clk100
<b>Sync</b>	
Sync Trigger Routing	PXI_Trig0
Commit Start Stop	

Figure 22 Parameters of multidevice sync



- Slot Number is the number marked on the top of the PXIe chassis. As shown in the figure below. Here we set Slot 2 as Master card, Slot 3 as Slave card.

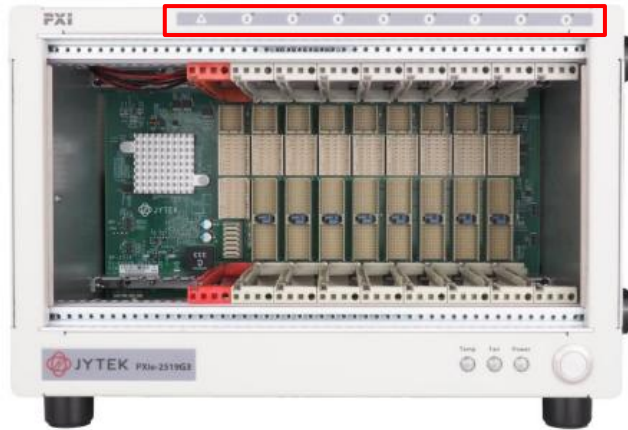


Figure 23 Slot number on PXIe Chassis

- Reference Clock set to **PXIe\_Clk100**
- Sync Trigger routing set to **PXI\_Trig0** or other trigger sources that are not in use.
- Click **commit** button, **Start** button will be enabled.

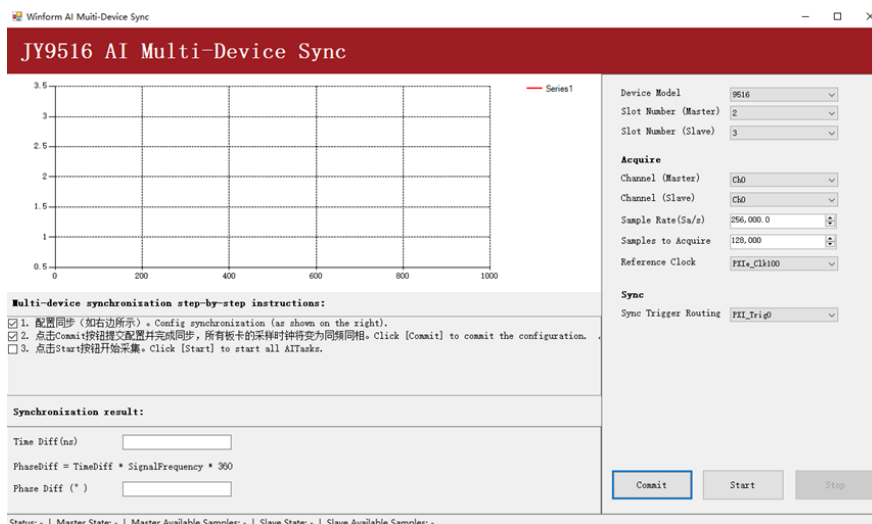


Figure 24 Result after click commit button

- Click **Start** button, the acquisition results, time differences and phase differences are shown in the figure below.

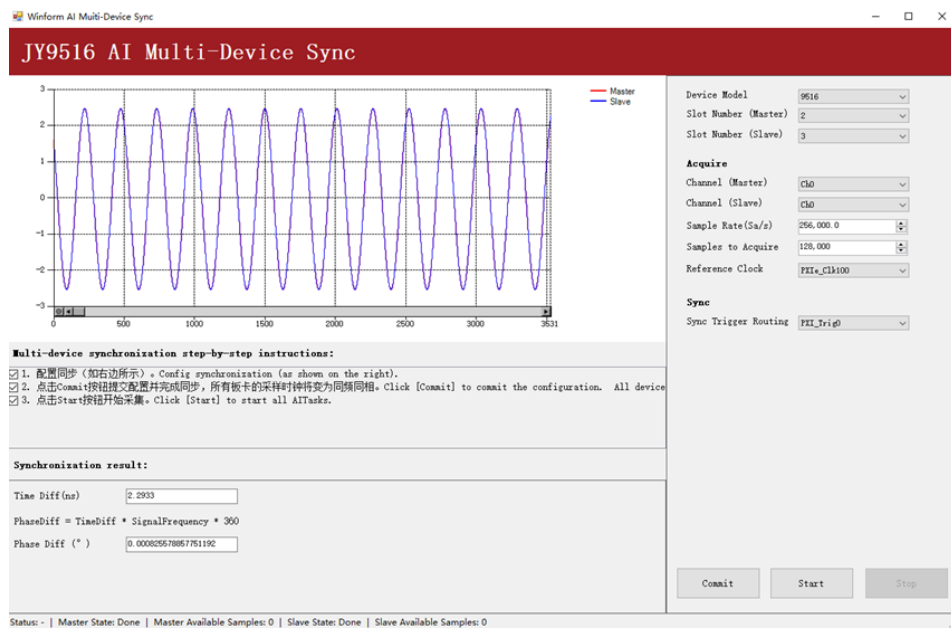


Figure 25 Acquisition result of multidevice sync

## 7. Additional Hardware Information

While JYTEK's default application platform is Visual Studio, the programming language is C#, we recognize there are other platforms that are either becoming very popular or have been widely used in the data acquisition applications. Among them are Python, C++ and LabVIEW. This chapter explains how you can use JY-9516 DSA module using one of this software.

### 7.1 Python

JYTEK provides and supports a native Python driver for JY-9516 boards. There are many different versions of Python. JYTEK has only tested in CPython version 3.5.4. There is no guarantee that JYTEK python drivers will work correctly with other versions of Python.

If you want to be our partner to support different Python platforms, please contact us.

### 7.2 C++

We recommend our customers to use C# drivers because C# platform deliver much better efficiency and performance in most situations. We also provide C++ drivers and examples in the Qt IDE, which can be downloaded from web. However, due to the limit of our resources, we do not actively support C++ drivers. If you want to be our partner to support C++ drivers, please contact us.

### 7.3 LabVIEW

LabVIEW is a software product from National Instruments. JYTEK does not support LabVIEW and will no longer provide LabVIEW interface to JY-9516 boards. Our third-party partners may have LabVIEW support to JY-9516 boards. We can recommend you if you want to convert your LabVIEW applications to C# based applications.

## 8. Calibration

JYTEK 9510 boards are precalibrated before the shipment. We recommend you recalibrate JY-9516 board periodically to ensure the measurement accuracy. A commonly accepted practice is one year. If you need to recalibrate your board, please contact JYTEK.

## 9. Appendix

### 9.1 Common Analog Measurement Issues

#### 9.1.1 DC, AC and DSA Mode

Figure 26 shows three different measurement modes: DC, AC and DSA. It is important to know what type of the measurement you are making. Table 21 shows differences and features in these three modes.

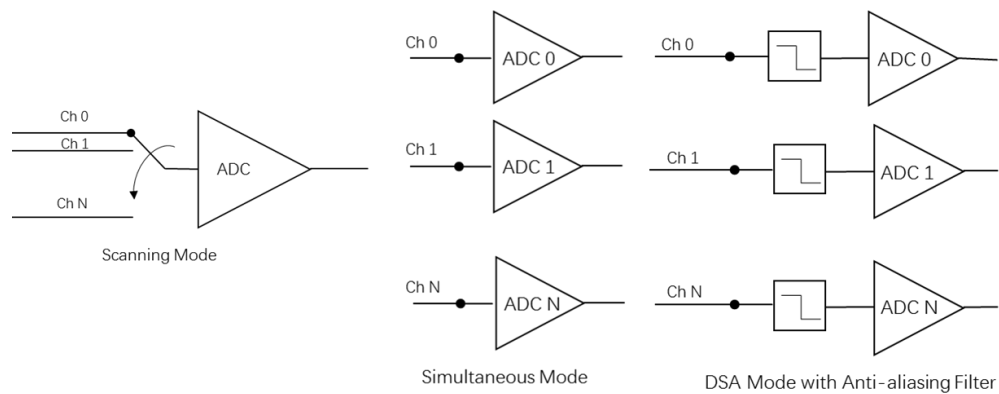


Figure 26 DC, AC and DSA Mode

	DC	AC	DSA
Signal Frequency (f)	$f=0$ , or $f \leq \epsilon \cdot f_s / 10$	$f_s > 5f$	$f_s > 2.5f$
Anti-aliasing Filter	No	No	Yes
Measurements			
Single point voltage accuracy	Yes	Maybe	No
Power Spectrum	No	Maybe	Yes
Rising/falling edges	No	Yes	No
Averaging	Time	Frequency	Frequency
ADC Mode			
Scanning	Optional	Optional	No
Scanning Interval (T)	$T \ll 1/f$	$T \ll 1/f$	N/A
Simultaneous	Optional	Optional	Yes
fs: channel sampling rate; $\epsilon$ : total accuracy;			

Table 21 DC, AC, DSA Measurements

## DC Mode

In a DC mode, the signal frequency  $f$  should be zero or very small. Many times, engineers use averaging to reduce the noise effect. But inappropriate use of averaging will not reduce the noise effect but introduce the error. Given the **Total Accuracy**  $\epsilon$ , from Sections 1.4, 1.5, 0, the maximum source signal frequency  $f$  should be bounded by:

$$f \leq \frac{\epsilon}{10} f_s$$

where  $f_s$  is the sample rate. This formula can be used in both the DAQ and the DS Mode. This formula suggests that a faster sampling device such as JY-9516 can allow bigger signal changes and still achieve excellent accuracy.

## AC Mode

The AC mode traditionally measures power line voltage of 50Hz or 60Hz, but has been extended to other frequencies. Due to the alternating nature of the AC signal, the average cannot be done in the time domain. If averaging must be used, it is used in the frequency domain when measuring the power spectrum.

Another use of the AC measurement is to analyze the signal's change. In this case, the sample rate must be sufficiently higher than the signal frequency to catch the changing nature of the signal. As a rule of thumb, 5 times of the signal frequency is often used.

## DSA Mode

The DSA (Dynamic Signal Analysis) mode mostly measures the signal frequency spectrum. In order to reduce the noise and increase the dynamic range, an anti-aliasing filter is used. Similar to the simultaneous mode, each channel is serviced by a dedicated ADC. To meet the sampling theorem, the sample rate  $f_s$  should be at least 2.5 times of the signal frequency.

## 9.2 DSA Measurement

### 9.2.1 Dynamic Signal Acquisition Concepts

#### Nyquist Frequency and Nyquist Bandwidth

Any sampling system, such as an ADC, is limited in the bandwidth of the signals it can measure. Specifically, a sampling rate of  $f_s$  can represent only signals with frequencies lower than  $f_s/2$ . This maximum frequency is known as the Nyquist frequency. The bandwidth from 0 Hz to the Nyquist frequency is the Nyquist bandwidth.

#### Noise

DSA devices typically have a dynamic range of more than 110 dB. Several factors can degrade the noise performance of input channels, such as noise picked up from nearby electronic devices. DSA devices work best when kept as far away as possible from other plug-in devices, power supplies, disk drives, and computer monitors. Cabling is also critical. Use well-shielded coaxial or floating cables for all connections. Route the cables away from sources of interference such as computer monitors, switching power supplies, and fluorescent lights. Physical motion or deformation can induce noise on sensitive analog cables. Use a transducer with a low output impedance to minimize system susceptibility to external noise sources and crosstalk.

You can reduce the effects of noise on your measurements by carefully choosing the sample rate to maximize the effectiveness of the anti-alias filtering. Computer monitor noise, for example, typically occurs at frequencies between 15 kHz and 65 kHz. If the signal of interest is restricted to below 10 kHz, for example, the anti-alias filters reject the monitor noise outside the frequency band of interest, and a sampling rate of at least 21.6 kS/s guarantees that any signal components in the 10 kHz bandwidth of interest are acquired without aliasing and without being attenuated by the digital filter. Refer to Analog Input Filters for more information about anti-alias filtering.

When possible, use the differential configuration to minimize the effect of any noise produced by ground currents in the chassis and common-mode noise. If you have particularly noisy AC power, consider external filtering, such as a line conditioner or an uninterruptible power supply.

***Notice:*** Electromagnetic interference can adversely affect the measurement accuracy of the DSA products described in this document. The inputs and outputs of these products are not connected to chassis ground for functional reasons. Therefore, the

*outer conductor of any connected coaxial cable is not connected to chassis ground and the outer conductor will not act as a shield for unwanted noise. The shield can act as an antenna to transmit noise into the environment or receive noise from the environment that could affect measurement accuracy. To ensure proper shielding effectiveness of connected coaxial cables, the outer conductor must be directly connected to chassis or earth ground at the load end of the cable. In addition, snap-on ferrite beads or other remedial measures may be required to prevent unwanted emissions or immunity. Refer to the specifications of your product for more information about EMC performance.*

---

### **Anti-Alias Filters**

A digitizer or ADC might sample signals containing frequency components above the Nyquist limit. The undesirable effect of the digitizer modulating out-of-band components into the Nyquist bandwidth is aliasing. The greatest danger of aliasing is that you cannot determine whether aliasing occurred by looking at the ADC output. If an input signal contains several frequency components or harmonics, some of these components might be represented correctly while others contain aliased artifacts.

Lowpass filtering to eliminate components above the Nyquist frequency either before or during the digitization process can guarantee that the digitized data set is free of aliased components. DSA devices employ both digital and analog lowpass filters to achieve this protection.

The delta-sigma ADCs on DSA devices include an oversampled architecture and sharp digital filters with cut-off frequencies that track the sampling rate. Thus, the filter automatically adjusts to follow the Nyquist frequency.

### **9.2.2 Dynamic Signal Acquisition Fundamentals**

#### **Accuracy and Flatness**

##### **What is Flatness?**

Under ideal conditions, an amplitude measurement's accuracy will not depend on the input signal's frequency. However, due to the non-ideal characteristics of real measurement devices, the measured amplitude of a signal can vary slightly according

to its frequency. Analog Input (AI) flatness is a measure of how a device's measurement response varies across its bandwidth. A perfect instrument would measure a 1 Vpk sine wave as exactly 1 Vpk regardless of the frequency of the sine wave as long as it was within the passband. However, no instrument is perfect and you will always see some amplitude variation with frequency.

The AI Flatness specification provided for DSA products tells you how much variation you can expect to see relative to the device's measurement at 1 kHz. AI Flatness is a relative accuracy specification. It indicates gain error you may see in addition to the Gain Accuracy specification (which is also relative to 1 kHz and is provided in our specification documents). If you wanted to know the absolute Gain error across the full measurement bandwidth, you would need to add the AI Flatness to the AI Gain Amplitude Accuracy specification.

In order to measure AI flatness, you would need a function generator capable of maintaining a very accurate sine wave amplitude across the bandwidth of interest (20 Hz to 20 kHz/45kHz/92.2kHz). If you sweep this function generator across the bandwidth, you could expect to measure the same amplitude +/- the specified AI Flatness in units of dB reference the amplitude of the signal at 1 kHz.

## **Dynamic Range**

### **What is Dynamic Range?**

The dynamic range of a device is the ratio of the largest and smallest signals that can be measured by circuit, normally expressed in dB.

$$\text{Dynamic Range in dB} = 20 * \log_{10}(V_{\text{max}} / V_{\text{min}})$$

In most cases, the full-scale input of a device is the largest signal that can be measured and the idle channel input noise determines the smallest signal that can be measured.

Dynamic range is a very important quantity to consider when choosing a DSA device. Oftentimes, DSA applications require the use of microphones and accelerometers-sensors that have very large dynamic ranges. Choosing an appropriate measurement device will allow you to take advantage of these sensors and the fullness of their range.

**Note:** When comparing dynamic range specifications between devices, it is very important to make sure that the measurement bandwidth, sample rate, input range



and input tone are identical. If any of these vary, the dynamic range comparison will be misleading.

### Distortion Specifications (THD, THD+N, SINAD)

When dealing with DSA hardware you are very likely to encounter a number of distortion related specifications. In order to understand these measurements, begin by taking a look at a typical Fast Fourier Transform (FFT) graph.

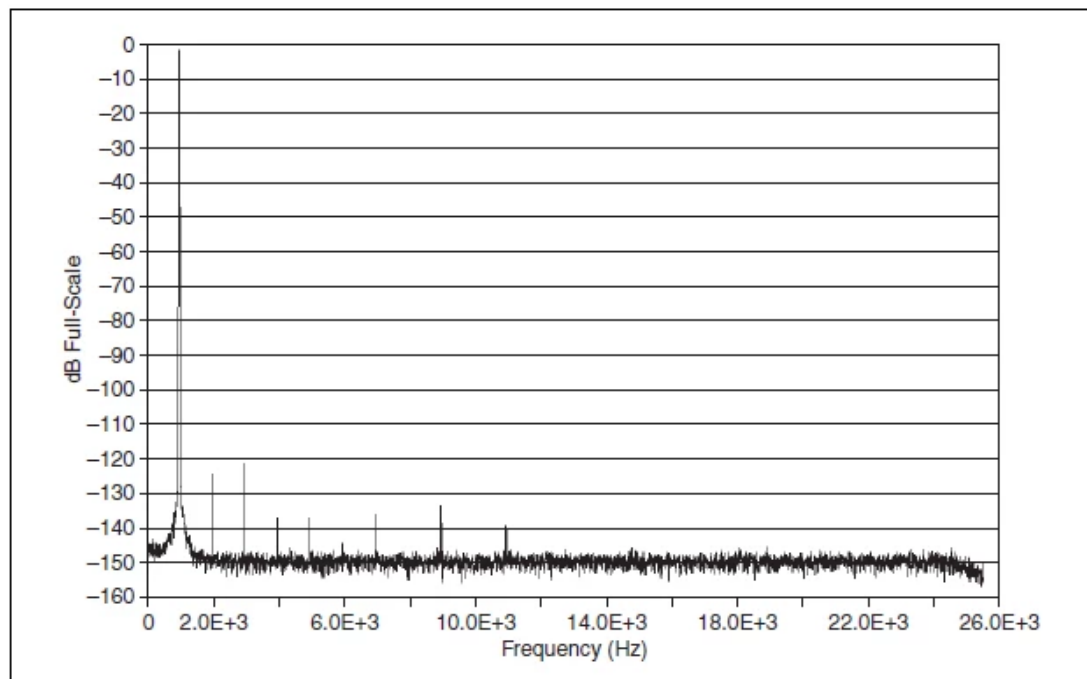


Figure 27: Typical FFT Plot with DSA device

This FFT was taken with a DSA device at a sample rate of 51.2 kS/s with a -1 dBFS (dB Full Scale) amplitude sine wave at 1kHz. There are several features of this FFT to consider when talking about distortion measurements:

1. The “fundamental” tone is the maximum peak in the FFT. In the figure below, this is the input tone at 1 kHz, colored green in the figure below.
2. After the fundamental tone, you can see a number of peaks at frequencies that are integer multiples of the “fundamental.” These peaks are called harmonic peaks because they are multiples of the fundamental, and are colored red in the figure below. The peak at 2 kHz is the second harmonic because it is the fundamental (1 kHz) times two. In this FFT, you can see the 2nd, 3rd, 4th, 5th, 6th, 7th, 9th, and 11th harmonics above the noise level.

3. After looking at the fundamental (highest peak) and harmonics (frequencies at integer multiples of the fundamental), the rest of the spectrum is called “noise.” The noise can be seen colored orange in the figure below.

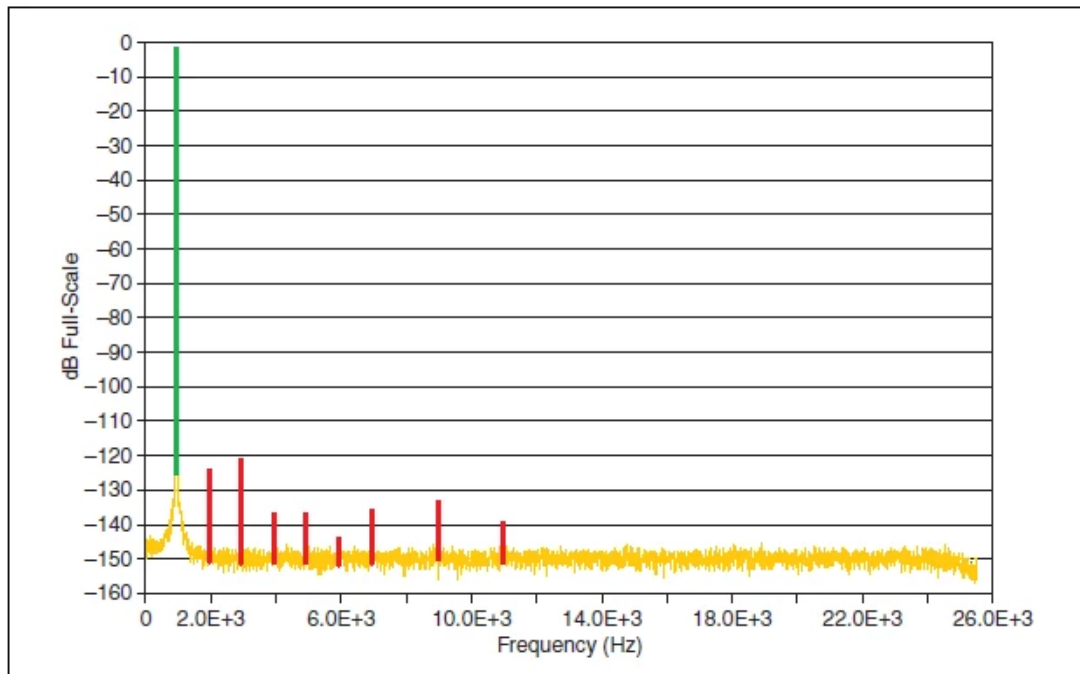


Figure 28: Color Coded FFT Plot

Distortion measurements can easily be illustrated using an FFT like the one in Figure 2. THD, THD+N and SINAD are different ratios of the power in these three illustrated signals (Fundamental, Harmonics and Noise).

#### ● THD or Total Harmonic Distortion

This is the total signal distortion due to harmonic signals. It can be defined as the ratio of the power in the harmonics divided by the power of the fundamental. Note that this measurement ignores the noise.

$$\text{THD} = \frac{\sum \text{Power (harmonics)}}{\text{Power (fundamental)}}$$

#### ● THD + N

This specification is the same as THD, but includes noise. You can think of THD+N as the total signal distortion due to harmonic signals and noise.

$$\text{THD} + \text{N} = \frac{\sum \text{Power (harmonics)} + \sum \text{Power (noise)}}{\text{Power (fundamental)}}$$

- **SINAD or the Signal to Noise and Distortion ratio**

The last of the common distortion measurements is SINAD. In this case, the “Signal” refers to the sum of fundamental, harmonics, and noise and "Distortion" refers to the sum of just the harmonics and noise, with the fundamental.

$$\text{SINAD} = (\text{Power (fundamental)} + \sum \text{Power (harmonics)} + \sum \text{Power (noise)}) / (\sum \text{Power (harmonics)} + \sum \text{Power (noise)})$$

### **Signal Aliasing**

When sampling signals at a given frequency,  $f_s$ , only frequency components less than or equal to half the sample rate will be represented correctly in an FFT ( $\leq f_s/2$ ). Signals with a frequency greater than  $f_s/2$  will be “aliased” back into the frequency band between 0 and  $f_s/2$ . If signal aliasing occurs, there is no way to tell in band (0 to  $f_s/2$ ) signals from out of band (greater than  $f_s/2$ ) signals.

In order to prevent signal aliasing and accurately represent the frequency content in the 0 to  $f_s/2$  band, DSA devices implement an oversampling architecture that allows for sample rate dependent filtering (as the sample rate changes, so will the cut off frequency of the filter). As a result, DSA devices have Bandwidth and Alias Rejection specifications that prevent signals from being aliased.

### **Synchronization**

Generally speaking, synchronization is important in DSA applications because it allows for accurate phase comparisons between channels in systems ranging from 2 to 10,000 channels. Phase comparisons are critical in many sound and vibration applications, including noise mapping. As channel count increases, more DSA devices will be required, and synchronizing these devices becomes necessary.

## **10. About JYTEK**

### **10.1 JYTEK China**

Founded in June, 2016, JYTEK China is a leading Chinese test & measurement company, providing complete software and hardware products for the test and measurement industry. The company has evolved from re-branding and reselling PXI(e) and DAQ products to a fully-fledged product company. The company offers complete lines of PXI, DAQ, USB products. More importantly, JYTEK has been promoting open-sourced based ecosystem and offers complete software products. Presently, JYTEK is focused on the Chinese market. Our Shanghai headquarters and production service center have regular stocks to ensure timely supply; we also have R&D centers in Xi'an and Chongqing. We also have highly trained direct technical sales representatives in Shanghai, Beijing, Tianjin, Xi'an, Chengdu, Nanjing, Wuhan, Guangdong, Haerbin, and Changchun. We also have many partners who provide system level support in various cities.

### **10.2 JYTEK Software Platform**

JYTEK has developed a complete software platform, SeeSharp Platform, for the test and measurement applications. We leverage the open sources communities to provide the software tools. Our platform software is also open sourced and is free, thus lowering the cost of tests for our customers. We are the only domestic vendor to offer complete commercial software and hardware tools.

### **10.3 JYTEK Warranty and Support Services**

With our complete software and hardware products, JYTEK is able to provide technical and sales services to wide range of applications and customers. In most cases, our products are backed by a 1-year warranty. For technical consultation, pre-sale and after-sales support, please contact JYTEK of your country.

## 11. Statement

The hardware and software products described in this manual are provided by JYTEK China, or JYTEK in short.

This manual provides the product review, quick start, some driver interface explanation for JYTEK JY-9516 Series of dynamic signal analyzer modules. The manual is copyrighted by JYTEK.

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While we try to keep this manual up to date, there are factors beyond our control that may affect the accuracy of the manual. Please check the latest manual and product information from our website.

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