

1. USB/PCIe/PXIe-9511 Specifications

Dynamic Signal Acquisition & Generation module



⌚ Please download <JYPEDIA>, you can quickly check the product price and main features.

Overview

The JY-9511 is a high-performance PXI analog I/O module designed for precision data acquisition and signal generation in dynamic measurement environments.

The analog input section offers four differential channels with 24-bit Delta-Sigma ADCs, supporting sampling rates up to 256 kS/s per channel. It accommodates input voltage ranges from ± 0.3125 V to ± 50 V, features AC/DC coupling options, and provides integrated IEPE excitation and TEDS compatibility, achieving a dynamic range of 111 dB.

The analog output section includes two channels utilizing 24-bit Delta-Sigma DACs, delivering precise signal generation with update rates up to 204.8 kS/s per channel and a dynamic range of 117 dB.

Engineered for versatility, the JY-9511 excels in applications such as vibration analysis, acoustic testing, structural health monitoring, and other dynamic signal measurement tasks, offering engineers and researchers superior data accuracy and reliability within PXI-based test systems.

1.1 Main Features

AI Features:

- 0.01 dB AI AC accuracy
- 24 bits resolution Synchronous acquisition
- 4 AI channels with simultaneous measurement
- AI Sampling rate: 62.5 S/s ~ 256 kS/s
- Voltage Range: ± 0.3125 V to ± 50 V
- Dynamic Range: 111 dB
- Antialiasing filters for accurate signal capture
- Software-configurable AC/DC coupling per channel
- 4 mA IEPE excitation per AI channel
- Transducer Electronic Data Sheet (TEDS) Support
- Analog/Digital/Software triggering for flexible operation
- AI Low distortion: THD -110 dBc

AO Features:

- 2 AO channels for signal generation
- AO Update rate: 100 S/s ~ 204.8 kS/s
- Voltage Range: ± 0.316 V to ± 10 V
- Dynamic Range: 117 dB
- AO Low distortion: THD -108 dBc

1.2 Input Characteristic

1.2.1 Analog Input

Analog input channels	4 ch
Input configuration	differential/Pseudo differential
Input coupling	AC/DC,selectable per channel
ADC resolution	24 bits
ADC type	Delta-sigma
Sample rate range	62.5S/s - 256 kS/s
Onboard memory	256MB for analog inputs
Transfer mode	Scatter-Gather DMA data transfer

Table 1 Input Characteristic

1.2.2 Input Signal Range

Range (V)	Vrms (Sine Input)
±0.3125	0.221
±0.625	0.442
±1.25	0.88
±2.5	1.77
±5	3.54
±10	7.07
±25	17.7
±50	35.4

Table 2 Input Signal Range

1.2.3 Common-Mode Range

Range (V)	Input	Configuration	
		Differential (Vp - Vn)*	PseudoDifferential (V peak)*
±10, ±5, ±2.5, ±1.25, ±0.625, ±0.3125	Positive input (+)	±12	±12
	Negative input (-)	±12	7 Vrms with Peaks ≤ 10
±50, ±25	Positive input (+)	±50	±50
	Negative input (-)	±50	7 Vrms with Peaks ≤ 10

*Voltages with respect to ground

Table 3 Common-Mode Range

1.2.4 Analog Input Overvoltage Protection

Positive terminal overvoltage protection	$\pm 60V$
Negative terminal overvoltage protection	7 Vrms with $ Peaks \leq 10V$ Pseudo differential $\pm 60V$ differential

Table 4 Analog Input Overvoltage Protection

1.3 AI Accuracy

1.3.1 Analog Input DC Accuracy

Range (V)	Residual Gain Error (PPM of Reading)	Residual Offset Error (PPM of Range)	INL Error (PPM of Range)
± 0.3125	210	140	55
± 0.625	260	160	20
± 1.25	250	160	20
± 2.5	240	160	20
± 5	240	160	30
± 10	250	160	30
± 25	230	120	610
± 50	280	160	610

Table 5 Analog Input Accuracy

1.3.2 Analog Input AC Accuracy

Specifications valid at any attenuation setting with a 1 kHz output signal.

$\pm 0.01dB$

1.4 Input Amplifier Characteristics

1.4.1 Input Impedance

	Configuration	
Input Impedance	Differential	Pseudodifferential
Between positive input and ground	$1 M\Omega$	$1 M\Omega$

Between negative input and ground	1 M Ω	58 Ω
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Table 6 Input Impedance

1.4.2 Input Common-Mode Rejection Ratio (CMRR)

Range (V)	Differential Configuration	
	DC-Coupled CMRR(dBc) $f_{in} \leq 1\text{kHz}$	AC-Coupled CMRR(dBc) $f_{in}=50\text{ or }60\text{ Hz}$
± 0.3125	101	68
± 0.625	102	68
± 1.25	100	68
± 2.5	95	68
± 5	89	67
± 10	87	67
± 25	58	61
± 50	58	60

Table 7 Common-Mode Rejection Ratio (CMRR)

1.5 AI Dynamic Characteristics

1.5.1 AI Bandwidth and Alias Rejection

-3 dB Bandwidth(Normal)	0.433*Fs
Aliasing Free Bandwidth(Normal)	0.4*Fs
Aliasing Free Bandwidth(Wide Bandwidth)	0.4535*Fs

Table 8 AI Bandwidth and Alias Rejection

1.5.2 AI Filter Delay

Normal Mode	
Sample Rate (kS/s)	Filter Delay(sample)
$32 < fs \leq 256$	38.00
$4 < fs \leq 32$	33.38
$0.0625 \leq fs \leq 4$	32.88
Wide Bandwidth Mode	
Sample Rate (kS/s)	Filter Delay(sample)
$32 < fs \leq 128$	48.00
$4 < fs \leq 32$	33.38
$0.0625 \leq fs \leq 4$	32.88

Table 9 AI Filter Delay

1.5.3 AI Coupling

-3 dB cutoff frequency	0.4 Hz
-0.1 dB cutoff frequency	4.5 Hz

Table 10 AI Coupling

1.5.4 AI Flatness

Range (V)	DC-Coupled Flatness (dB)	
	20 Hz to 20 kHz	20 Hz to 100 kHz
± 0.3125	0.006	0.05
± 0.625	0.006	0.05
± 1.25	0.006	0.05
± 2.5	0.006	0.05
± 5	0.006	0.05
± 10	0.007	0.10
± 25	0.130	0.26
± 50	0.130	0.26

Table 11 AI Flatness

1.5.5 AI Interchannel Phase Mismatch

Range (V)	DC-Coupled Mismatch (deg)		AC-Coupled Mismatch (deg)
	20 Hz to 20 kHz	20 Hz to 100 kHz	20 Hz
±0.3125	0.184	0.757	0.038
±0.625	0.167	0.696	0.035
±1.25	0.144	0.575	0.035
±2.5	0.141	0.546	0.035
±5	0.146	0.581	0.034
±10	0.143	1.701	0.035
±25	1.866	1.909	0.034
±50	1.864	1.893	0.033

Table 12 AI Interchannel Phase Mismatch

1.5.6 AI Idle Channel Noise

Range (V)	Noise(µVrms)	
	$f_s = 51.2 \text{ kS/s}$ (22.1kHz bandwidth)	$f_s = 256 \text{ kS/s}$ (110 kHz bandwidth)
±0.3125	2.1	4.5
±0.625	2.3	5.3
±1.25	3.2	7.3
±2.5	5.2	12.5
±5	9.8	23.7
±10	19.0	46.3
±25	72.8	150.6
±50	110.0	252.9

Table 13 AI Idle Channel Noise

1.5.7 AI Spectral Noise Density

Range (V)	Noise Density at 1 kHz (nV/ $\sqrt{\text{Hz}}$)
± 0.3125	14
± 0.625	16
± 1.25	21
± 2.5	35
± 5	65
± 10	126
± 25	500
± 50	750

Table 14 AI Spectral Noise Density

1.5.8 AI Dynamic Range

Range (V)	AI Dynamic Range(dBFS)	
	$1 \text{ kS/s} \leqslant f_s \leqslant 51.2 \text{ kS/s}$	$51.2 \text{ kS/s} \leqslant f_s \leqslant 256 \text{ kS/s}$
± 0.3125	101	94
± 0.625	106	99
± 1.25	109	102
± 2.5	111	103
± 5	111	103
± 10	111	104
± 25	108	101
± 50	110	103

Table 15 AI Dynamic Range

1.5.9 AI Spurious Free Dynamic Range (SFDR)

Range (V)	SFDR (dBc)
±0.3125	106
±0.625	109
±1.25	108
±2.5	112
±5	110
±10	107
±25	111
±50	110

fs = 204.8 kS/s
1 kHz input tone, input amplitude is the lesser of -1 dBFS or 8.91 Vpk
Measurement includes all harmonics.
Preliminary specifications

Table 16 AI Spurious Free Dynamic Range (SFDR)

1.5.10 AI Total Harmonic Distortion (THD), Balanced Source

Range (V)	THD (dBc)
±0.3125	-103
±0.625	-107
±1.25	-106
±2.5	-110
±5	-107
±10	-107
±25	-109
±50	-108

fs = 204.8 kS/s
1 kHz input tone, input amplitude is the lesser of -1 dBFS or 8.91 Vpk
Measurement includes all harmonics.
Preliminary specifications

Table 17 AI Total Harmonic Distortion (THD), Balanced Source

1.5.11 AI THD+N, Unbalanced Source

Range (V)	THD+N(dBc)	
	51.2kS/s	256kS/s
±0.3125	-88	-86
±0.625	-94	-92
±1.25	-98	-96
±2.5	-100	-98
±5	-103	-100

1 kHz input tone.
Input amplitude is the lesser of -1 dBFS .
Preliminary specifications

Table 18 AI THD+N, Unbalanced Source

1.5.12 AI Crosstalk (Input Channel Separation)

Range (V)	Crosstalk for Adjacent Channels (dBc)	
	1 kHz	92.1 kHz
±0.3125	-150	-115
±0.625	-150	-115
±1.25	-150	-115
±2.5	-150	-115
±5	-150	-115
±10	-150	-115
±25	-96	-64
±50	-96	-64

Source impedance $\leq 50 \Omega$
Input amplitude is the lesser of -1 dBFS or 8.91 Vpk

Table 19 AI Crosstalk (Input Channel Separation)

1.6 Output Characteristic

1.6.1 Analog Output

Analog output channels	2
D/A converter (DAC) resolution	24 bits
DAC type	Delta-sigma
Update rates (fs) range	100S/s~204.8 kS/s*
Output configuration	Differential or pseudodifferential (50 Ω between negative output and chassis ground), each channel independently software-selectable
Output voltage full-scale range	±10.0 V peak : 0dB, 7.07 V RMS (sine output) ±3.16 V peak : -10dB, 2.24 V RMS (sine output) ±1 V peak : -20dB, 0.707 V RMS (sine output) ±0.316 V peak : -30dB, 0.224 V RMS (sine output)
Output load	600 Ω, minimum/warranted
Overvoltage Protection	±60V
Onboard memory	256MB for analog output
Trigger Type	Digital/Software
Trigger Mode	Rising-edge or falling-edge
Operating Temperature	0 °C~ 55 °C
Output coupling	DC
Short circuit protection	Indefinite protection between positive and negative
Minimum working load	600 Ω
*When the sampling rate of AO is between [125Hz, 204.8KHz], it can work with AI as long as their sampling rates are in a power-of-2 relationship. However, when the sampling rate of AO is between [100Hz, 125Hz], it cannot work with AI.	

Table 20 Analog Output

1.6.2 DAC modulator oversample rate

Sample Rate	DAC modulator oversample rate
$100\text{S/s} \leq \text{fs} \leq 400\text{S/s}$	32768 fs
$400\text{S/s} < \text{fs} \leq 800\text{S/s}$	16384 fs
$0.8\text{kS/s} < \text{fs} \leq 1.6\text{ kS/s}$	8192 fs
$1.6\text{ kS/s} < \text{fs} \leq 3.2\text{ kS/s}$	4096 fs
$3.2\text{ kS/s} < \text{fs} \leq 6.4\text{ kS/s}$	2048 fs
$6.4\text{ kS/s} < \text{fs} \leq 12.8\text{ kS/s}$	1024 fs
$12.8\text{ kS/s} < \text{fs} \leq 25.6\text{ kS/s}$	512 fs
$25.6\text{ kS/s} < \text{fs} \leq 51.2\text{ kS/s}$	256 fs
$51.2\text{ kS/s} < \text{fs} \leq 102.4\text{ kS/s}$	128 fs
$102.4\text{ kS/s} < \text{fs} \leq 204.8\text{ kS/s}$	64 fs

Table 21 DAC modulator oversample rate

1.6.3 Output Direct Digital Synthesizer (DDS) Mode

UpdateRate	Signal frequency resolution
$128\text{K} < \text{fs} \leq 204.8\text{K}$	$\text{fs} * 128 / 65536$
$102.4\text{K} < \text{fs} \leq 128\text{K}$	$\text{fs} * 256 / 65536$

Table 22 Output Signal Range

1.6.4 Output Signal Range

Range (V)	Attenuation (dB)*	V RMS (Sine Output)
± 0.316	30	0.224
± 1.0	20	0.707
± 3.16	10	2.24
± 10.0	0	7.07

*Each output channel attenuation is independently software selectable

Table 23 Output Signal Range

1.6.5 Analog Output Overvoltage Protection

Output Terminals	Short-Circuit Duration	Overvoltage (V peak), Minimum/Warranted
AO+ to chassis GND	Indefinite	±60
AO- to chassis GND	Indefinite	±60
AO+ to AO-	Indefinite	±60

Table 24 Analog Output Overvoltage Protection

1.7 AO Accuracy

1.7.1 Analog Output DC Accuracy

Range (V)	Residual Gain Error (PPM of Reading)	Residual Offset Error (PPM of Range)	INL Error (PPM of Range)
±0.316	4200	210	610
±1	4000	100	720
±3.16	3900	120	250
±10	3900	130	470

Table 25 Analog Output Accuracy

1.7.2 Analog Output AC Accuracy

Specifications valid at any attenuation setting with a 1 kHz output signal: ±0.04dB

1.8 AO Dynamic Characteristics

1.8.1 AO Bandwidth and Image Rejection

Image rejection	62 dB min (Fin > 768 kHz)
-3 dB BW	0.49 fs

Table 26 AO Bandwidth and Image Rejection

1.8.2 AO Filter Delay

Sample Rate (kS/s)	Filter Delay (Samples)
100 S/s \leq fs \leq 400 S/s	33.3
400 S/s < fs \leq 800 S/s	33.3
0.8 kS/s < fs \leq 1.6 kS/s	33.5
1.6 kS/s < fs \leq 6.4 kS/s	33.8
6.4 kS/s < fs \leq 12.8 kS/s	35.6
12.8 kS/s < fs \leq 51.2 kS/s	37.8
51.2 kS/s < fs \leq 204.8 kS/s	59.0

Table 27 AO Filter Delay

1.8.3 AO Interchannel Phase Mismatch

All attenuation settings (deg)	
20 Hz to 20 kHz	0.12
20 Hz to 92.1 kHz	0.48

Table 28 AO Interchannel Phase Mismatch

1.8.4 AO Idle Channel Noise

Range (V)	Noise(μ Vrms)	
	102.5 kS/s (30kHz Bandwidth)	204.8 kS/s (80kHz Bandwidth)
± 0.316	8.8	14.9
± 1	8.8	14.9
± 3.16	9.0	15.1
± 10	10.4	17.3

Table 29 AO Idle Channel Noise

1.8.5 AO Dynamic Range

Range (V)	102.5 kS/s (30kHz Bandwidth)	204.8 kS/s (80kHz Bandwidth)
± 0.316	88	84
± 1	98	94
± 3.16	108	103
± 10	117	112

Table 30 AO Dynamic Range

1.8.6 AO Spurious Free Dynamic Range (SFDR)

Range (V)	SFDR (dBc)
±0.316	100
±1	107
±3.16	110
±10	108

fs = 204.8 kS/s
1 kHz output frequency, -1 dBFS output amplitude
Measurement includes all harmonics.

Table 31 AO Spurious Free Dynamic Range (SFDR)

1.8.7 AO Total Harmonic Distortion (THD)

Range (V)	THD (dBc)
±0.316	-99
±1	-106
±3.16	-108
±10	-107

fs = 204.8 kS/s
1 kHz output frequency, -1 dBFS output amplitude
Measurement includes all harmonics.

Table 32 AO Total Harmonic Distortion (THD)

1.8.8 AO THD+N

Range (V)	THD+N
±0.316	-83
±1	-93
±3.16	-98
±10	-102

fs = 204.8 kS/s
1 kHz output frequency, -1 dBFS output amplitude
Measurement includes all harmonics.

Table 33 AO THD+N

1.8.9 AO Crosstalk (Output to Input Channel)

Range(V)	Crosstalk (dBc)	
	1kHz	80kHz
±0.3125	-154	-114
±0.625	-155	-114
±1.25	-154	-114
±2.5	-155	-114
±5	-155	-114
±10	-150	-114
±25	-113	-83
±50	-113	-83

Table 34 AO Crosstalk (Output to Input Channel Separation)

1.8.10 AO Crosstalk (Output to Output Channel)

All attenuation settings (0, 20, and 40 dB)	
1 kHz signal	-150
92.1 kHz signal	-112

Table 35 AO Crosstalk (Output Channel Separation)

1.9 Integrated Electronic Piezoelectric (IEPE)

Current 4 mA ±10%	each channel independently software selectable
Compliance	<p>32 V min</p> <p>Vcom + Vbias + Vfull-scale must be 0 to 32 V</p> <p>Vcommon-mode is the common-mode voltage seen by the input channel</p> <p>Vbias is the DC bias voltage of the sensor</p> <p>Vfull-scale is the AC full-scale voltage of the sensor</p>

Table 36 Integrated Electronic Piezoelectric (IEPE)

1.10 Transducer Electronic Data Sheet (TEDS)

Supports Transducer Electronic Data Sheet (TEDS) according to the IEEE 1451 Standard: Class I, all module inputs.

1.11 Time Base

Internal reference clock	Accuracy	± 1 ppm, over operating temperature range
	Aging	1 ppm in first year
External reference clock (only PXIe-9511)	Clock source	PXIe-100MHz
	Frequency	100 MHz
	Accuracy	Depende on PXI backplane

Table 37 time base

External time base: Equal to accuracy of external time base

1.12 Bus Interface

Bus support	PXIe
Synchronization(PXIe)	CLK_100

Table 38 Bus Interface

1.13 Power Requirements

+3.3 V	3.0 A, maximum, maximum/warranted
+12 V	2.0 A, maximum, maximum/warranted

Table 39 Power Requirements

1.14 Triggers

Trigger Type	Analog / Digital / Software
Analog Trigger Voltage Range	Software Programmable
Trigger Mode	Start / Reference / ReTrigger
Digital Trigger Source	PFIO
Digital Trigger Compatibility	3.3V TTL, 5V tolerant
Interval of ReTrigger	5 Samples
As a input:	
Digital Input Impedance	50kΩ
Digital Input Logic Low	VIL Min : 0 / Max : 1.0 V
Digital Input Logic High	VIH Min : 2 V / Max : 5.3 V
As a output:	
Digital Output Logic Low	0 V, IOL Max: 24 mA
Digital Output Logic High :	2.6 V ~ 3.3 V, IOH Max: -24 mA
Digital Output Impedance	50Ω

Table 40 Triggers

1.15 Physical

Dimensions	Standard 3U PXI
Weight	0.23 kg

Table 41 Physical

1.16 Connector



Figure 1 PXIe-9511 Front Panel



Signal	Con0	Signal	Cable	Function
GND		G1	GND	
	S2 S1	CLK IN	CH7	RSV
GND		G2	GND	
	S4 S3	PIFO	CH6	PFI0
AO1-		G3	GND	
	S6 S5	AO1+	CH5	AO1
AO0-		G4	GND	
	S8 S7	AO0+	CH4	AO0
AI3-		G5	GND	
	S10 S9	AI3+	CH3	AI3
AI2-		G6	GND	
	S12 S11	AI2+	CH2	AI2
AI1-		G7	GND	
	S14 S13	AI1+	CH1	AI1
AI0-		G8	GND	
	S16 S15	AI0+	CH0	AI0
		G9	GND	

Figure 2 PXIe-9511 Connector

PIN number	Infiniband Cable	9511 Function
G1		CGND
S1	CH7_P	RSV
S2	CH7_N	GND
G2		CGND
S3	CH6_P	PFIO
S4	CH6_N	CGND
G3		CGND
S5	CH5_P	AO1_P
S6	CH5_N	AO1_N
G4		CGND
S7	CH4_P	AO0_P
S8	CH4_N	AO0_N
G5		CGND
S9	CH3_P	AI3_P
S10	CH3_N	AI3_N
G6		CGND
S11	CH2_P	AI2_P
S12	CH2_N	AI2_N
G7		CGND
S13	CH1_P	AI1_P
S14	CH1_N	AI1_N
G8		CGND
S15	CH0_P	AI0_P
S16	CH0_N	AI0_N
G9		CGND

Table 42 Pin Definition

1.17 Special Operating Restriction

The amplitude of the out-of-band signal between 0.3M and 3MHz must be less than 20% of full scale.¹

1. *This restriction does not affect applications where PXIe-9511 is connected to the front-end sensors such as microphones and accelerometers because these sensors have built-in attenuation so that the out-of-band voltage will not exceed 20% of full scale. If you have question on this restriction, please contact JYTEK for more information.*

1.18 Optimizing Precision: Custom Gain Error Calibration for Fixed Sampling Rates

The gain error of the 9511 model varies with different sampling rates, and the specifications provided in this manual cover the error range across all potential sampling rates.

If users calibrate the gain error of their acquisition card for their specific sampling rate, they can achieve an accuracy that surpasses the general specifications that encompass all sampling rates.

2. Order Information

- PXIe-9511 (PN: JY5859082-01)
256 kS/s, 24-Bit, 4-Input / 204.8 kS/s, 24-Bit 2-Output PXIe Dynamic Signal Acquisition & Generation module
- PCIe-9511 (PN: JY7255307-01)
256 kS/s, 24-Bit, 4-Input / 204.8 kS/s, 24-Bit 2-Output PCIe Dynamic Signal Acquisition & Generation module
- USB-9511 (PN: JY4499908-01)
256 kS/s, 24-Bit, 4-Input / 204.8 kS/s, 24-Bit 2-Output USB Dynamic Signal Acquisition & Generation module
- Accessory
ACL-2000802-02 (PN: JY2000802-02)
20 cm, 8-CH shielded x4 InfiniBand to BNC cable

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4. Software

4.1 System Requirements

JY-9511 boards can be used in a Windows or a Linux operating system.

Microsoft Windows: Windows 7 32/64 bit, Windows 10 32/64 bit.

Linux Kernel Versions: There are many Linux versions. It is not possible JYTEK can support and test our devices under all different Linux versions. JYTEK will at the best support the following Linux versions.

Linux Version
Ubuntu LTS
16.04: 4.4.0-21-generic(desktop/server)
16.04.6: 4.15.0-45-generic(desktop) 4.4.0-142-generic(server)
18.04: 4.15.0-20-generic(desktop) 4.15.0-91-generic(server)
18.04.4: 5.3.0-28-generic (desktop) 4.15.0-91-generic(server)
Localized Chinese Version
中标麒麟桌面操作系统软件（兆芯版）V7.0（Build61）:3.10.0-862.9.1.nd7.zx.18.x86_64
中标麒麟高级服务器操作系统软件V7.0U6:3.10.0-957.el7.x86_64

Table 43 Supported Linux Versions

4.2 System Software

When using the JY-9511 in the Window environment, you need to install the following software from Microsoft website:

Microsoft Visual Studio Version 2015 or above,

.NET Framework version is 4.0 or above.

.NET Framework is coming with Windows 10. For Windows 7, please check .NET Framework version and upgrade to 4.0 or later version.

Given the resources limitation, JYTEK only tested JY-9511 be with .NET Framework 4.0 with Microsoft Visual Studio 2015. JYTEK relies on Microsoft to maintain the compatibility for the newer versions.

4.3 C# Programming Language

All JYTEK default programming language is Microsoft C#. This is Microsoft recommended programming language in Microsoft Visual Studio and is particularly suitable for the test and measurement applications. C# is also a cross platform programming language.

4.4 JY-9511 Series Hardware Driver

After installing the required application development environment as described above, you need to install the JY-9511 hardware driver.

JYTEK hardware driver has two parts: the shared common driver kernel software (FirmDrive) and the specific hardware driver.

Common Driver Kernel Software (FirmDrive): FirmDrive is the JYTEK's kernel software for all hardware products of JYTEK instruments. You need to install the FirmDrive software before using any other JYTEK hardware products. FirmDrive only needs to be installed once. After that, you can install the specific hardware driver.

Specific Hardware Driver: Each JYTEK hardware has a C# specific hardware driver. This driver provides rich and easy-to-use C# interfaces for users to operate various JY-9511 function. JYTEK has standardized the ways which JYTEK and other vendor's DSA modules are used by providing a consistent user interface, using the methods, properties and enumerations in the object-oriented programming environment. Once you get yourself familiar with how one JYTEK DAQ card works, you should be able to know how to use all other DAQ hardware by using the same methods.

Note that this driver does not support cross-process, and if you are using more than one function, it is best to operate in one process.

4.5 Install the SeeSharpTools from JYTEK

To efficiently and effectively use JY-9511 boards, you need to install a set of free C# utilities, SeeSharpTools from JYTEK. The SeeSharpTools offers rich user interface functions you will find convenient in developing your applications. They are also needed to run the examples come with JY-9511 hardware. Please register and download the latest SeeSharpTools from our website, www.jytek.com.

4.6 Running C# Programs in Linux

Most C# written programs in Windows can be run by MonoDevelop development system in a Linux environment. You would develop your C# applications in Windows using Microsoft Visual Studio. Once it is done, run this application in the MonoDevelop environment. This is JYTEK recommended way to run your C# programs in a Linux environment.

If you want to use your own Linux development system other than MonoDevelop, you can do it by using our Linux driver. However, JYTEK does not have the capability to support the Linux applications. JYTEK completely relies upon Microsoft to maintain the cross-platform compatibility between Windows and Linux using MonoDevelop.

5. JYPEDIA

JYPEDIA is an excel file. It contains JYTEK product information, pricing, inventory information, drivers, software, technical support, knowledge base etc. You can register and download a [JYPEDIA](#) excel file from our web www.jytek.com. JYTEK highly recommends you use this file to obtain information from JYTEK.

6. Using JY-9511 in Other Software

While JYTEK's default application platform is Visual Studio, the programming language is C#, we recognize there are other platforms that are either becoming very popular or have been widely used in the data acquisition applications. Among them are Python, C++ and LabVIEW. This chapter explains how you can use JY-9511 DSA module using one of this software.

6.1 Python

JYTEK provides and supports a native Python driver for JY-9511 boards. There are many different versions of Python. JYTEK has only tested in CPython version 3.5.4. There is no guarantee that JYTEK python drivers will work correctly with other versions of Python.

If you want to be our partner to support different Python platforms, please contact us.

6.2 C++

We recommend our customers to use C# drivers because C# platform deliver much better efficiency and performance in most situations. We also provide C++ drivers and examples in the Qt IDE, which can be downloaded from web. However, due to the limit of our resources, we do not actively support C++ drivers. If you want to be our partner to support C++ drivers, please contact us.

6.3 LabVIEW

LabVIEW is a software product from National Instruments. JYTEK does not support LabVIEW and will no longer provide LabVIEW interface to JY-9511 boards. Our third-party partners may have LabVIEW support to JY-9511 boards. We can recommend you if you want to convert your LabVIEW applications to C# based applications.

7. Calibration

JYTEK 9510 boards are precalibrated before the shipment. We recommend you recalibrate JY-9511 board periodically to ensure the measurement accuracy. A commonly accepted practice is one year. If you need to recalibrate your board, please contact JYTEK.

8. Appendix

8.1 Common Analog Measurement Issues

8.1.1 DC, AC and DSA Mode

Figure 3 shows three different measurement modes: DC, AC and DSA. It is important to know what type of the measurement you are making. Table 44 shows differences and features in these three modes.

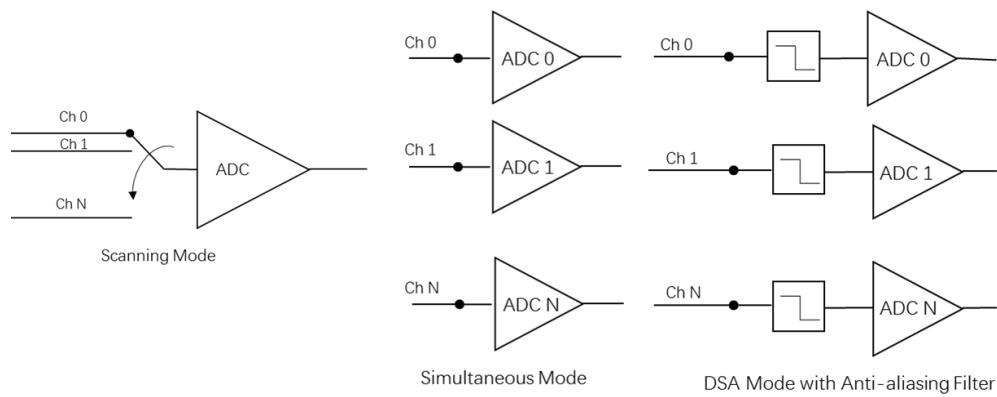


Figure 3 DC, AC and DSA Mode

	DC	AC	DSA
Signal Frequency (f)	$f=0$, or $f \leq \varepsilon * f_s / 10$	$f_s > 5f$	$f_s > 2.5f$
Anti-aliasing Filter	No	No	Yes
Measurements			
Single point voltage accuracy	Yes	Maybe	No
Power Spectrum	No	Maybe	Yes
Rising/falling edges	No	Yes	No
Averaging	Time	Frequency	Frequency
ADC Mode			
Scanning	Optional	Optional	No
Scanning Interval (T)	$T \ll 1/f$	$T \ll 1/f$	N/A
Simutaneous	Optional	Optional	Yes

f_s : channel sampling rate; ε : total accuracy;

Table 44 DC, AC, DSA Measurements

DC Mode

In a DC mode, the signal frequency f should be zero or very small. Many times, engineers use averaging to reduce the noise effect. But inappropriate use of averaging will not reduce the noise effect but introduce the error. Given the **Total Accuracy ε** , from Sections 1.5, the maximum source signal frequency f should be bounded by:

$$f \leq \frac{\varepsilon}{10} f_s$$

where f_s is the sample rate. This formula can be used in both the DAQ and the DS Mode. This formula suggests that a faster sampling device such as JY-9511 can allow bigger signal changes and still achieve excellent accuracy.

AC Mode

The AC mode traditionally measures power line voltage of 50Hz or 60Hz, but has been extended to other frequencies. Due to the alternating nature of the AC signal, the average cannot be done in the time domain. If averaging must be used, it is used in the frequency domain when measuring the power spectrum.

Another use of the AC measurement is to analyze the signal's change. In this case, the sample rate must be sufficiently higher than the signal frequency to catch the changing nature of the signal. As a rule of thumb, 5 times of the signal frequency is often used.

DSA Mode

The DSA (Dynamic Signal Analysis) mode mostly measures the signal frequency spectrum. In order to reduce the noise and increase the dynamic range, an anti-aliasing filter is used. Similar to the simultaneous mode, each channel is serviced by a dedicated ADC. To meet the sampling theorem, the sample rate f_s should be at least 2.5 times of the signal frequency.

8.2 DSA Measurement

8.2.1 Dynamic Signal Acquisition Concepts

Nyquist Frequency and Nyquist Bandwidth

Any sampling system, such as an ADC, is limited in the bandwidth of the signals it can measure. Specifically, a sampling rate of f_s can represent only signals with frequencies lower than $f_s/2$. This maximum frequency is known as the Nyquist frequency. The bandwidth from 0 Hz to the Nyquist frequency is the Nyquist bandwidth.

Noise

DSA devices typically have a dynamic range of more than 110 dB. Several factors can degrade the noise performance of input channels, such as noise picked up from nearby electronic devices. DSA devices work best when kept as far away as possible from other plug-in devices, power supplies, disk drives, and computer monitors. Cabling is also critical. Use well-shielded coaxial or floating cables for all connections. Route the cables away from sources of interference such as computer monitors, switching power supplies, and fluorescent lights. Physical motion or deformation can induce noise on sensitive analog cables. Use a transducer with a low output impedance to minimize system susceptibility to external noise sources and crosstalk.

You can reduce the effects of noise on your measurements by carefully choosing the sample rate to maximize the effectiveness of the anti-alias filtering. Computer monitor noise, for example, typically occurs at frequencies between 15 kHz and 65 kHz. If the signal of interest is restricted to below 10 kHz, for example, the anti-alias filters reject the monitor noise outside the frequency band of interest, and a sampling rate of at least 21.6 kS/s guarantees that any signal components in the 10 kHz bandwidth of interest are acquired without aliasing and without being attenuated by the digital filter. Refer to Analog Input Filters for more information about anti-alias filtering.

When possible, use the differential configuration to minimize the effect of any noise produced by ground currents in the chassis and common-mode noise. If you have particularly noisy AC power, consider external filtering, such as a line conditioner or an uninterruptible power supply.

Notice: *Electromagnetic interference can adversely affect the measurement accuracy of the DSA products described in this document. The inputs and outputs of these products are not connected to chassis ground for functional reasons. Therefore, the*

outer conductor of any connected coaxial cable is not connected to chassis ground and the outer conductor will not act as a shield for unwanted noise. The shield can act as an antenna to transmit noise into the environment or receive noise from the environment that could affect measurement accuracy. To ensure proper shielding effectiveness of connected coaxial cables, the outer conductor must be directly connected to chassis or earth ground at the load end of the cable. In addition, snap-on ferrite beads or other remedial measures may be required to prevent unwanted emissions or immunity. Refer to the specifications of your product for more information about EMC performance.

Anti-Alias Filters

A digitizer or ADC might sample signals containing frequency components above the Nyquist limit. The undesirable effect of the digitizer modulating out-of-band components into the Nyquist bandwidth is aliasing. The greatest danger of aliasing is that you cannot determine whether aliasing occurred by looking at the ADC output. If an input signal contains several frequency components or harmonics, some of these components might be represented correctly while others contain aliased artifacts.

Lowpass filtering to eliminate components above the Nyquist frequency either before or during the digitization process can guarantee that the digitized data set is free of aliased components. DSA devices employ both digital and analog lowpass filters to achieve this protection.

The delta-sigma ADCs on DSA devices include an oversampled architecture and sharp digital filters with cut-off frequencies that track the sampling rate. Thus, the filter automatically adjusts to follow the Nyquist frequency.

8.2.2 Dynamic Signal Acquisition Fundamentals

Accuracy and Flatness

What is Flatness?

Under ideal conditions, an amplitude measurement's accuracy will not depend on the input signal's frequency. However, due to the non-ideal characteristics of real measurement devices, the measured amplitude of a signal can vary slightly according

to its frequency. Analog Input (AI) flatness is a measure of how a device's measurement response varies across its bandwidth. A perfect instrument would measure a 1 Vpk sine wave as exactly 1 Vpk regardless of the frequency of the sine wave as long as it was within the passband. However, no instrument is perfect and you will always see some amplitude variation with frequency.

The AI Flatness specification provided for DSA products tells you how much variation you can expect to see relative to the device's measurement at 1 kHz. AI Flatness is a relative accuracy specification. It indicates gain error you may see in addition to the Gain Accuracy specification (which is also relative to 1 kHz and is provided in our specification documents). If you wanted to know the absolute Gain error across the full measurement bandwidth, you would need to add the AI Flatness to the AI Gain Amplitude Accuracy specification.

In order to measure AI flatness, you would need a function generator capable of maintaining a very accurate sine wave amplitude across the bandwidth of interest (20 Hz to 20 kHz/45kHz/92.2kHz). If you sweep this function generator across the bandwidth, you could expect to measure the same amplitude +/- the specified AI Flatness in units of dB reference the amplitude of the signal at 1 kHz.

Dynamic Range

What is Dynamic Range?

The dynamic range of a device is the ratio of the largest and smallest signals that can be measured by circuit, normally expressed in dB.

$$\text{Dynamic Range in dB} = 20 * \log_{10}(V_{\text{max}} / V_{\text{min}})$$

In most cases, the full-scale input of a device is the largest signal that can be measured and the idle channel input noise determines the smallest signal that can be measured.

Dynamic range is a very important quantity to consider when choosing a DSA device. Oftentimes, DSA applications require the use of microphones and accelerometers-sensors that have very large dynamic ranges. Choosing an appropriate measurement device will allow you to take advantage of these sensors and the fullness of their range.

Note: When comparing dynamic range specifications between devices, it is very important to make sure that the measurement bandwidth, sample rate, input range

and input tone are identical. If any of these vary, the dynamic range comparison will be misleading.

Distortion Specifications (THD, THD+N, SINAD)

When dealing with DSA hardware you are very likely to encounter a number of distortion related specifications. In order to understand these measurements, begin by taking a look at a typical Fast Fourier Transform (FFT) graph.

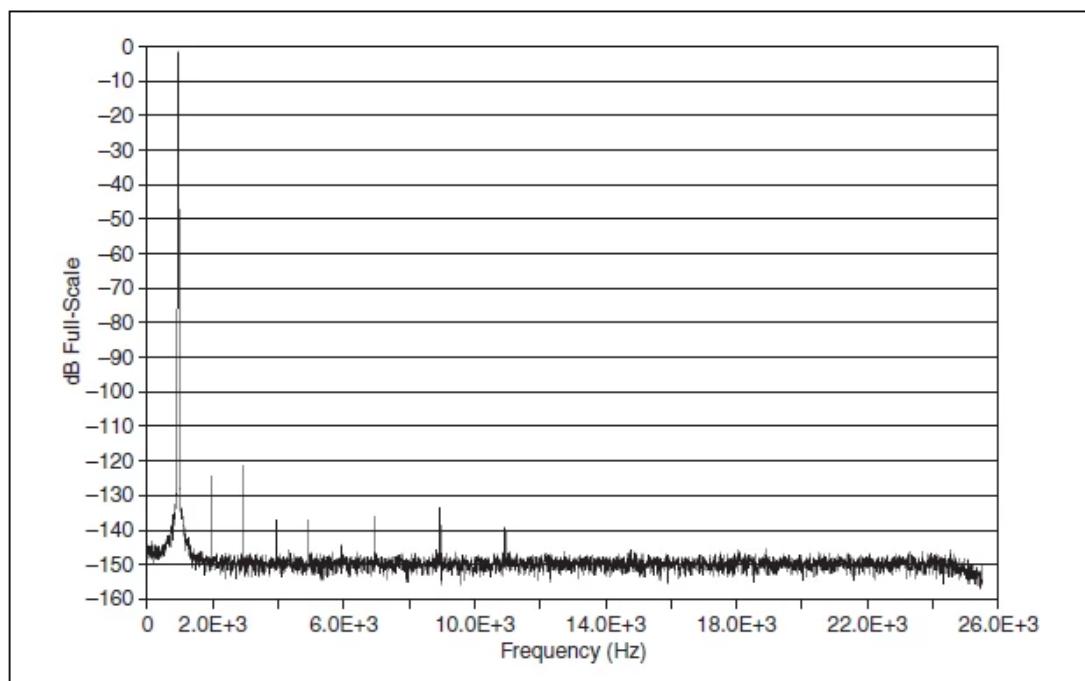


Figure 4: Typical FFT Plot with DSA device

This FFT was taken with a DSA device at a sample rate of 51.2 kS/s with a -1 dBFS (dB Full Scale) amplitude sine wave at 1kHz. There are several features of this FFT to consider when talking about distortion measurements:

1. The “fundamental” tone is the maximum peak in the FFT. In the figure below, this is the input tone at 1 kHz, colored green in the figure below.
2. After the fundamental tone, you can see a number of peaks at frequencies that are integer multiples of the “fundamental.” These peaks are called harmonic peaks because they are multiples of the fundamental, and are colored red in the figure below. The peak at 2 kHz is the second harmonic because it is the fundamental (1 kHz) times two. In this FFT, you can see the 2nd, 3rd, 4th, 5th, 6th, 7th, 9th, and 11th harmonics above the noise level.

- After looking at the fundamental (highest peak) and harmonics (frequencies at integer multiples of the fundamental), the rest of the spectrum is called “noise.” The noise can be seen colored orange in the figure below.

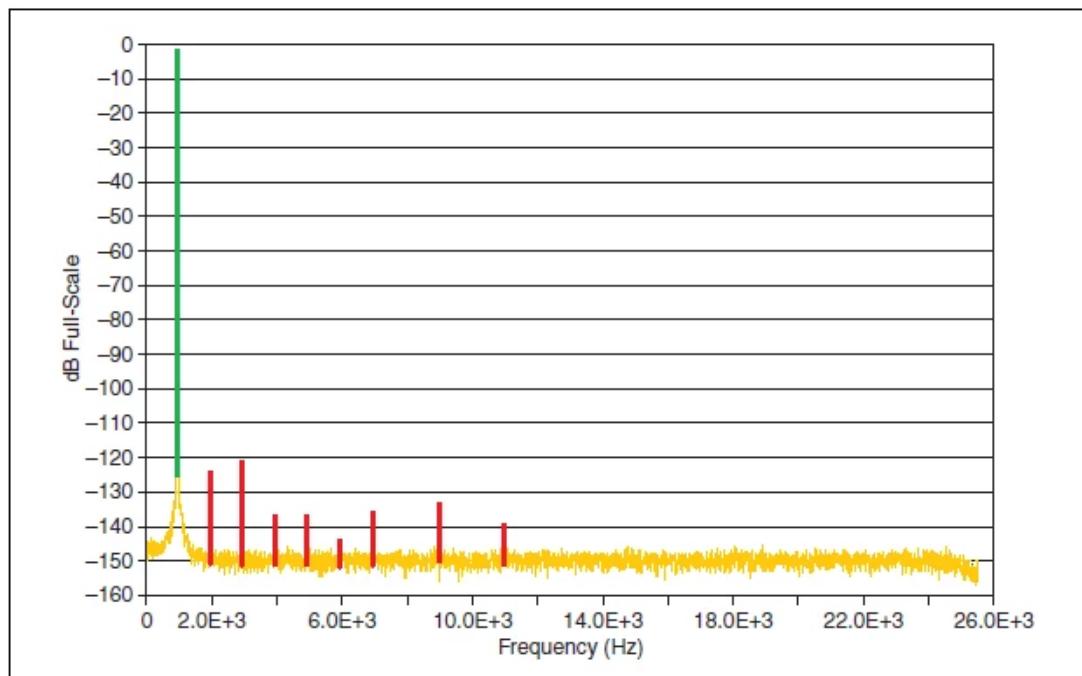


Figure 5: Color Coded FFT Plot

Distortion measurements can easily be illustrated using an FFT like the one in Figure 2. THD, THD+N and SINAD are different ratios of the power in these three illustrated signals (Fundamental, Harmonics and Noise).

● THD or Total Harmonic Distortion

This is the total signal distortion due to harmonic signals. It can be defined as the ratio of the power in the harmonics divided by the power of the fundamental. Note that this measurement ignores the noise.

$$\text{THD} = \sum \text{Power (harmonics)} / \text{Power (fundamental)}$$

● THD + N

This specification is the same as THD, but includes noise. You can think of THD+N as the total signal distortion due to harmonic signals and noise.

$$\text{THD} + \text{N} = \sum \text{Power (harmonics)} + \sum \text{Power (noise)} / \text{Power (fundamental)}$$

- **SINAD or the Signal to Noise and Distortion ratio**

The last of the common distortion measurements is SINAD. In this case, the "Signal" refers to the sum of fundamental, harmonics, and noise and "Distortion" refers to the sum of just the harmonics and noise, with the fundamental.

$$\text{SINAD} = (\text{Power (fundamental)} + \sum \text{Power (harmonics)} + \sum \text{Power (noise)}) / (\sum \text{Power (harmonics)} + \sum \text{Power (noise)})$$

Signal Aliasing

When sampling signals at a given frequency, f_s , only frequency components less than or equal to half the sample rate will be represented correctly in an FFT ($\leq f_s/2$). Signals with a frequency greater than $f_s/2$ will be "aliased" back into the frequency band between 0 and $f_s/2$. If signal aliasing occurs, there is no way to tell in band (0 to $f_s/2$) signals from out of band (greater than $f_s/2$) signals.

In order to prevent signal aliasing and accurately represent the frequency content in the 0 to $f_s/2$ band, DSA devices implement an oversampling architecture that allows for sample rate dependent filtering (as the sample rate changes, so will the cut off frequency of the filter). As a result, DSA devices have Bandwidth and Alias Rejection specifications that prevent signals from being aliased.

Synchronization

Generally speaking, synchronization is important in DSA applications because it allows for accurate phase comparisons between channels in systems ranging from 2 to 10,000 channels. Phase comparisons are critical in many sound and vibration applications, including noise mapping. As channel count increases, more DSA devices will be required, and synchronizing these devices becomes necessary.

9. About JYTEK

9.1 JYTEK China

Founded in June, 2016, JYTEK China is a leading Chinese test & measurement company, providing complete software and hardware products for the test and measurement industry. The company has evolved from re-branding and reselling PXI(e) and DAQ products to a fully-fledged product company. The company offers complete lines of PXI, DAQ, USB products. More importantly, JYTEK has been promoting open-sourced based ecosystem and offers complete software products. Presently, JYTEK is focused on the Chinese market. Our Shanghai headquarters and production service center have regular stocks to ensure timely supply; we also have R&D centers in Xi'an and Chongqing. We also have highly trained direct technical sales representatives in Shanghai, Beijing, Tianjin, Xi'an, Chengdu, Nanjing, Wuhan, Guangdong, Haerbin, and Changchun. We also have many partners who provide system level support in various cities.

9.2 JYTEK Software Platform

JYTEK has developed a complete software platform, SeeSharp Platform, for the test and measurement applications. We leverage the open sources communities to provide the software tools. Our platform software is also open sourced and is free, thus lowering the cost of tests for our customers. We are the only domestic vendor to offer complete commercial software and hardware tools.

9.3 JYTEK Warranty and Support Services

With our complete software and hardware products, JYTEK is able to provide technical and sales services to wide range of applications and customers. In most cases, our products are backed by a 1-year warranty. For technical consultation, pre-sale and after-sales support, please contact JYTEK of your country.

10. Statement

The hardware and software products described in this manual are provided by JYTEK China, or JYTEK in short.

This manual provides the product review, quick start, some driver interface explanation for JYTEK JY-9511 Series of dynamic signal analyzer modules. The manual is copyrighted by JYTEK.

No warranty is given as to any implied warranties, express or implied, including any purpose or non-infringement of intellectual property rights, unless such disclaimer is legally invalid. JYTEK is not responsible for any incidental or consequential damages related to performance or use of this manual. The information contained in this manual is subject to change without notice.

While we try to keep this manual up to date, there are factors beyond our control that may affect the accuracy of the manual. Please check the latest manual and product information from our website.

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