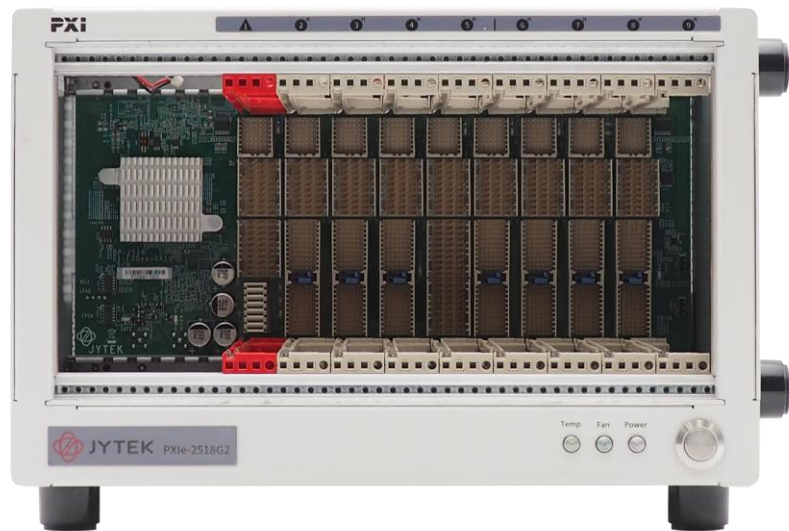




# PXIe-2518 Chassis

## User Manual



User Manual Version: 1.0.0

Revision Date: November 5, 2025

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# 1. Introduction

## 1.1 Overview

The PXIe-2518 is a high-performance, cost-effective 9-slot PXI/PXIe chassis. It complements JYTEK's PXIe-2518 9-slot model, which includes 7 hybrid slots and 1 PXI Express system timing slot. Featuring an updated mechanical design, it caters to customers looking to reduce system costs while maintaining high performance.

Depending on PCIe link speed capability, PXIe-2518 series provide two models as shown in Table 1.

Model Name	PCIe Link Speed Capability	System Bandwidth	Slot Bandwidth
PXIe-2518G3	Gen3	16 GB/s	4 GB/s
PXIe-2518G2	Gen2	8 GB/s	2 GB/s

Table 1 PXIe-2518 series model name

Note:

- system bandwidth defined as data rate between controller and chassis backplane.
- slot bandwidth defined as data rate between peripheral module and chassis backplane.

## 1.2 Main Features

- High data throughput 9-slot PCIe Gen2 (PXIe-2518G2) or Gen3 PXIe chassis (PXIe-2518G3)
- High clock accuracy  $\pm 1$  ppm and low phase jitter
- Support 10 MHz system reference clock in /out
- Low power ripple noise
- Specially designed for cost effective PXI/PXIe applications
- Ideal for OEM vendors

## 2. Hardware

### 2.1 Backplane Overview

#### 2.1.1 Backplane Architecture

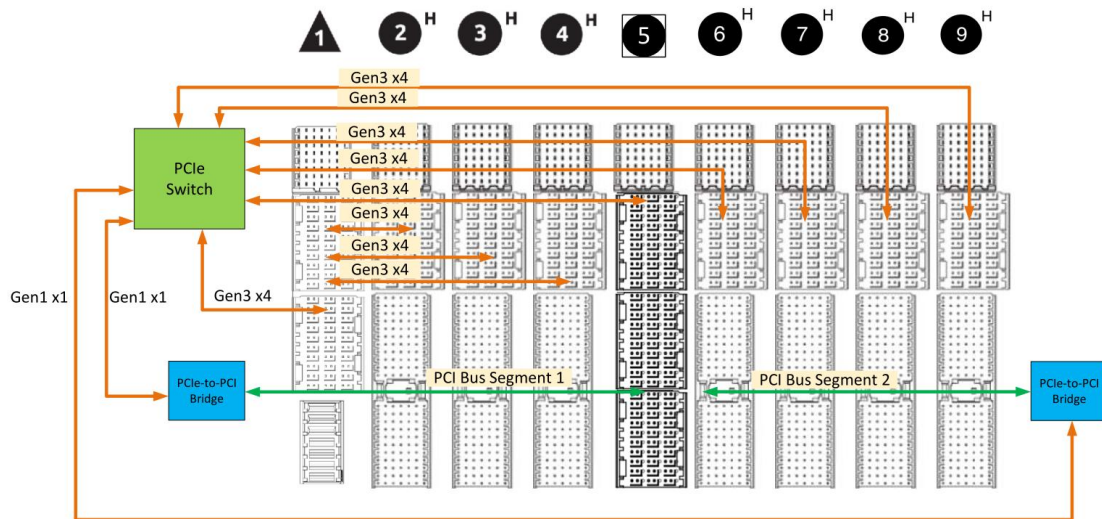


Figure 1 PXle-2518 Gen3 Backplane Architecture

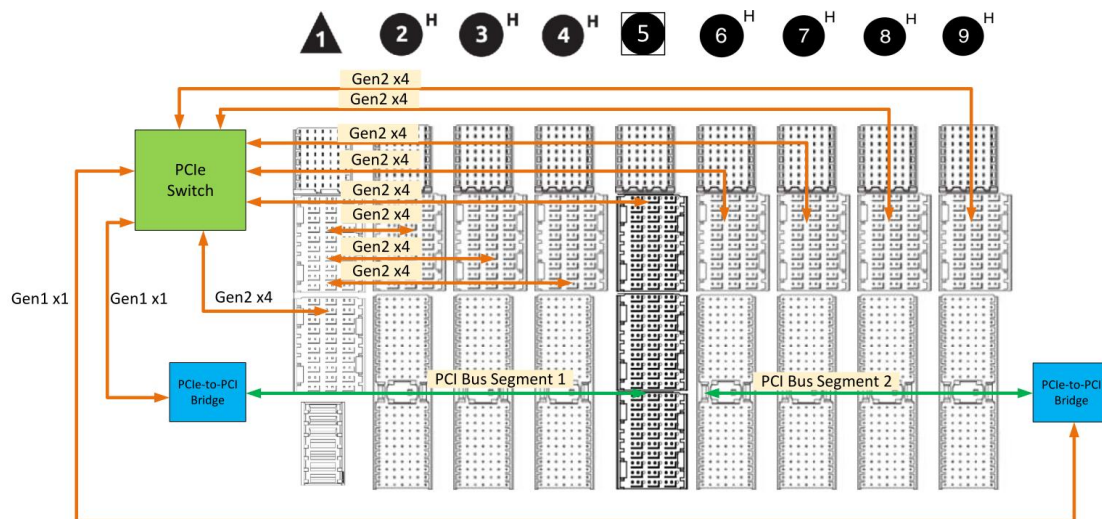


Figure 2 PXle-2518 Gen2 Backplane Architecture

#### 2.1.2 System Controller Slot

The System Controller slot is a fixed PCIe 4-Link configuration. Link 1, 2 and 3 are routed to slot2, slot3 and slot4 respectively. Link 4 is routed to PCIe switch and

downstream to slot5 ~ slot9 and PCI bus. The chassis can accommodate a maximum 4-slot width PXIe controller.

### 2.1.3 System Timing Slot

The System Timing slot, designated as Slot 10, provides one dedicated single-ended star trigger and three pairs of differential star trigger lines to each peripheral slot. The routing for the single-ended star trigger signals (PXI\_STAR) and differential star trigger signals (PXIe\_DSTAR) is as follows.

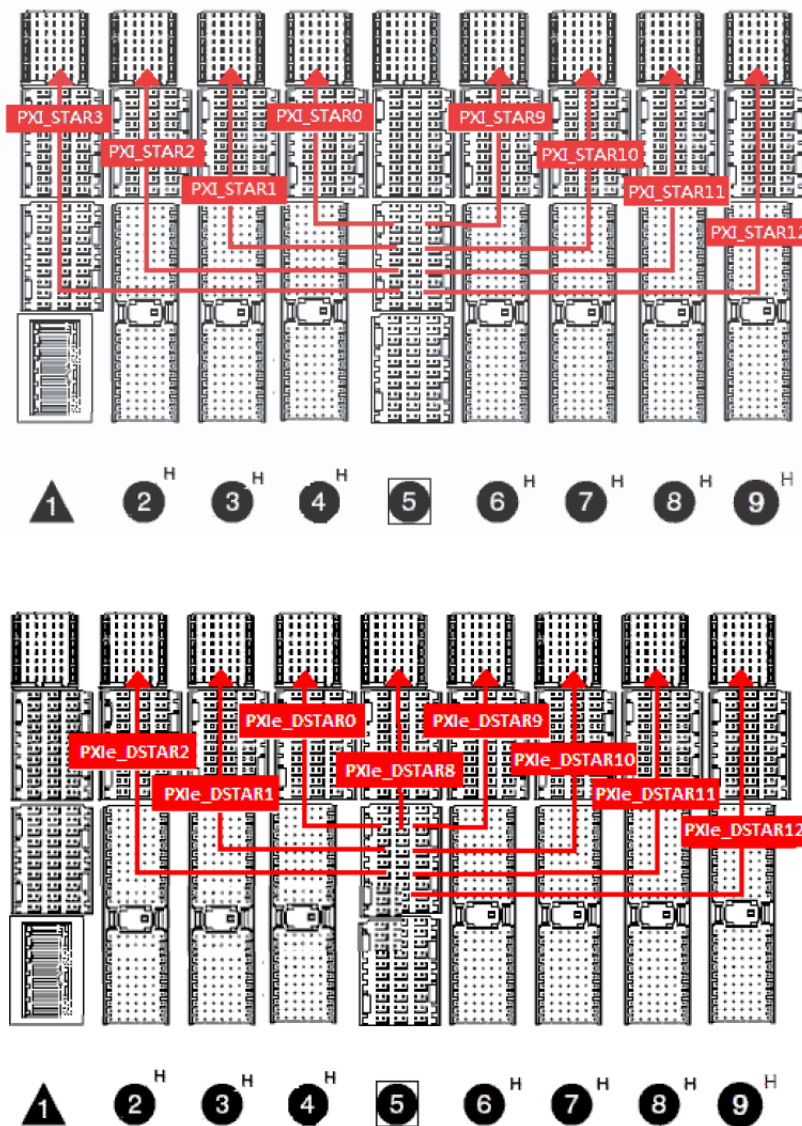


Figure 2 Star Trigger & Differential Star Bus Routing

Slot	PXI_Star	PXIe_DStar
1	3	N/A
2	2	2
3	1	1
4	0	0
5	N/A	8
6	9	9
7	10	10
8	11	11
9	12	12

Table 2 Star Trigger & Differential Star Bus Assignments

### 2.1.4 Peripheral Slot

PXIe-2518 provides eight hybrid peripheral slots. It can accept the following peripheral modules:

- PXI Express Peripheral Module
- CompactPCI Express Type-2 Peripheral Module
- Hybrid slot compatible PXI-1 Peripheral Module
- CompactPCI 32-bit Peripheral Module

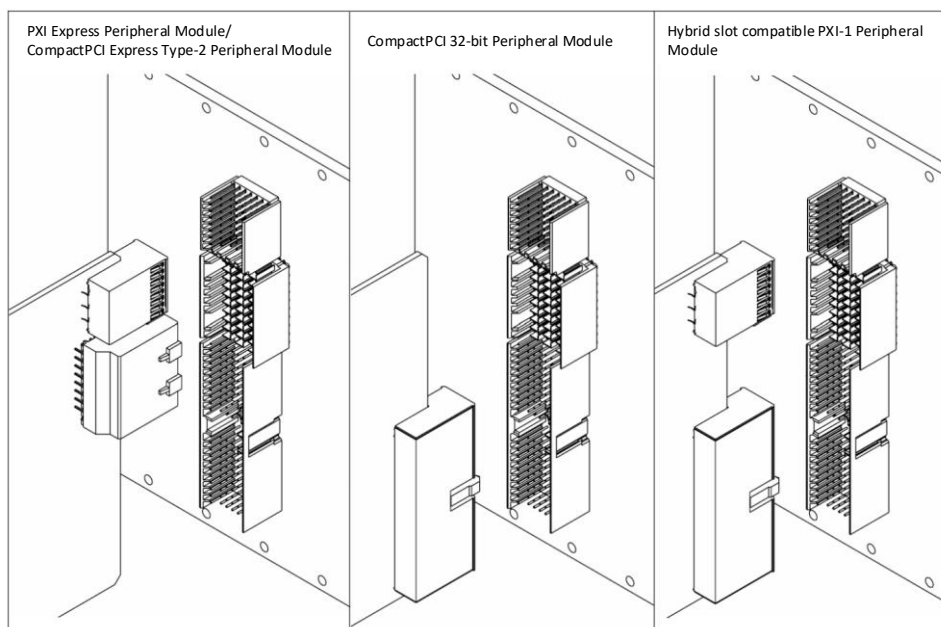


Figure 3 PXIe-2518 Peripheral Slot Compatible Modules

Each peripheral slot PCIe link can support Gen3 x4 (PXIe-2518G3) or Gen2 x4 (PXIe-2518G2), providing maximum single-direction bandwidth of 4GB/s or 2GB/s. And each



peripheral slot can also support 32bit PCB bus, providing maximum single-direction bandwidth of 132MB/s.

### 2.1.5 PXI Trigger Bus

All slots on PXIe-2518 share eight trigger lines, peripheral module can deliver trigger or clock via the trigger bus to synchronize the data acquisition operation.

### 2.1.6 PXI Local Bus

The local bus on PXIe-2518 is a daisy-chained bus that connects each peripheral slot with adjacent peripheral slots to the left and right, which by routing PXI Local Bus 6 signal between adjacent peripheral slots.

### 2.1.7 System Reference Clock and Synchronization Signal

The PXIe-2518 supplies 10MHz reference clock (PXI\_CLK10), 100MHz reference clock (PXIe\_CLK100) and synchronization signal (PXIe\_SYNC100) to each peripheral slot for inter-module synchronization.

The PXIe-2518 has the default timing relationship of PXI\_CLK10, PXIe\_CLK100 and PXIe\_SYNC100 as show in Figure 4 which comply with PXI-5 specification.

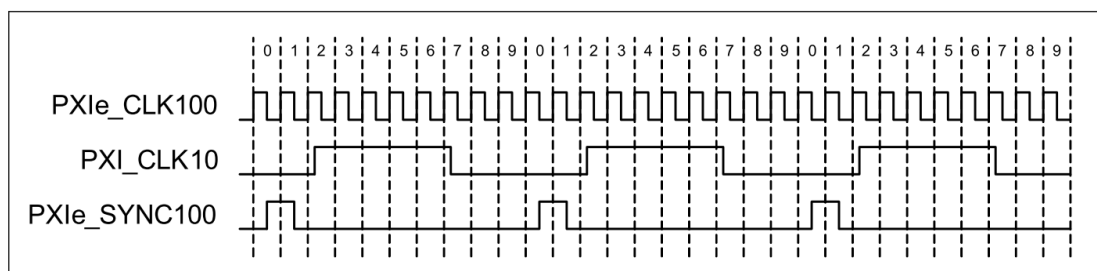


Figure 4 PXIe-2518 System Reference Clock Default Behavior

## 2.2 Specifications

### 2.2.1 Basic

Descriptions	PXIe-2518G3	PXIe-2518G2
PXI Chassis Type	PXIe	PXIe
Slot Count	9	9
Maximum slot bandwidth	4 GB/s (PCIe Gen3 x4)	2 GB/s (PCIe Gen2 x4 )
Maximum system bandwidth	16 GB/s (PCIe Gen3 x16)	8 GB/s (PCIe Gen2 x16)
Chassis Power Supply Type	AC	AC
Slot Cooling Capacity	58 W (0°C ~ 40°C) 38 W (0°C ~ 50°C)	58 W (0°C ~ 40°C) 38 W (0°C ~ 50°C)
Onboard Clock Type	TCXO	TCXO
External Clocking	Yes	Yes
Number of hybrid slots	7	7
Number of PXIe slots	0	0
Number of PXI slots	0	0
System timing slot	1	1
External Trigger Access	No	No
Redundant HW	No	No

Table 1 Basic Specification

### 2.2.2 Electrical

#### AC Input

Descriptions	PXIe-2518G2/G3
Total Chassis Power	850 W
Input voltage range	90 to 264 VAC
Input frequency	50~60 Hz
Input current rating	10~5 A
Efficiency	87% typical

## DC Output

Voltage Rail	Maximum Current	Load Regulation	Maximum Ripple and Noise (20 MHz BW)
+5V_AUX	4 A	±5%	50 mVpp
+12 V	62.5 A	±5%	120 mVpp
+5V	30 A	±5%	50 mVpp
+3.3V	26 A	±5%	50 mVpp
-12V	0.5 A	±5%	120 mVpp

Maximum total available power for the PXIe-2518G2/G3 is 750 W.

The maximum combined power available on +3.3 V and +5 V is 150 W.

## 2.2.3 System Synchronization Clock

### PXI\_CLK10

Maximum slot-to-slot skew	66 ps
Accuracy	±1 ppm max
Maximum jitter	3.7 ps RMS phase-jitter (10 Hz–1 MHz range)
Duty-factor	45%–55%
Unloaded signal swing	3.3 V ±0.3 V

### PXIe\_CLK100

Maximum slot-to-slot skew	80 ps
Accuracy	±1 ppm max
Maximum jitter	3.7 ps RMS phase-jitter (10 Hz–12 kHz range)
	95 fs RMS phase-jitter (12 kHz–20 MHz range)
Duty-factor	45%–55%
Absolute differential voltage	400–1000 mV

### PXIe\_SYNC100

Maximum slot-to-slot skew	66 ps
Accuracy	±1 ppm max

Maximum jitter	3.7 ps RMS phase-jitter (10 Hz–12 kHz range)
	4.8 ps RMS phase-jitter (12 kHz–20 MHz range)
Duty-factor	10%
Absolute differential voltage	400–1000 mV

Table 2 System Synchronization Clock

## 2.2.4 Continuous Current Capability

(at 50°C ambient temperature)

### System Controller Slot XJ1 Connector

+3.3 V	15 A
+5 V	15 A
+12 V	30 A
5 Vaux	1 A

### Hybrid Peripheral Slot XP4 Connector

+3.3 V	9A
+12 V	6 A
5 Vaux	1 A

### Hybrid Peripheral Slot P1 Connector

+3.3 V	6 A
+5 V	6 A
+12 V	1 A
-12 V	1 A
V (I/O)	11 A

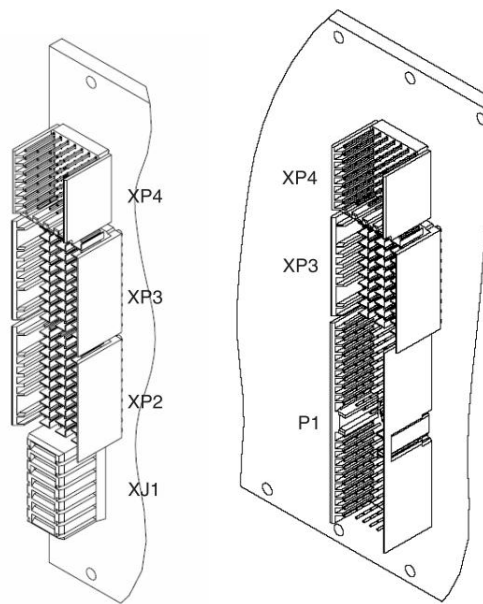


Table 3 Continuous Current Capability

## 2.2.5 Physical and Environment

### Operating Environment

Maximum altitude	5000 m
Ambient temperature range	0 to 50 °C
Relative humidity range	10 to 90%, noncondensing

### Storage Environment

Ambient temperature range	-20 °C to 80 °C
Relative humidity range	10% to 90%

Table 4 Environment

### Sound Pressure Level

Auto fan (up to ~30 °C ambient)	59 dBA
High fan	62 dBA

### Sound Power

Auto fan (up to ~30 °C ambient)	66 dBA
High fan	69 dBA

Table 5 Acoustic Emissions

Size	3 U
------	-----

Table 6 Backplane

Width	274.36 mm
Depth	306.7 mm
Height	175.4 mm
Weight	6.5 kg

Table 7 Chassis Size and Weight

## 2.3 Mechanical Dimensions

All dimensions are shown in mm (millimeters)

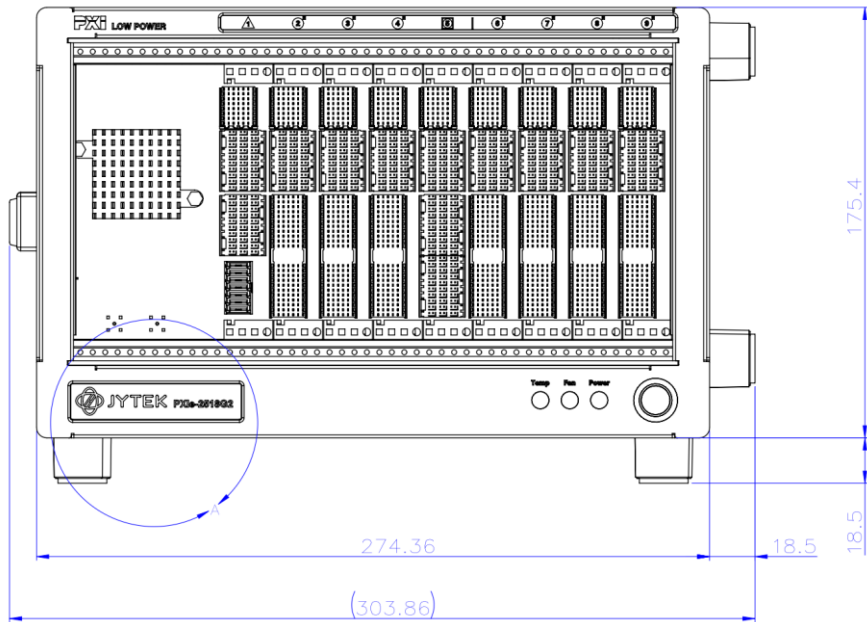


Figure 3 Front View (PXle-2518G3/G2)

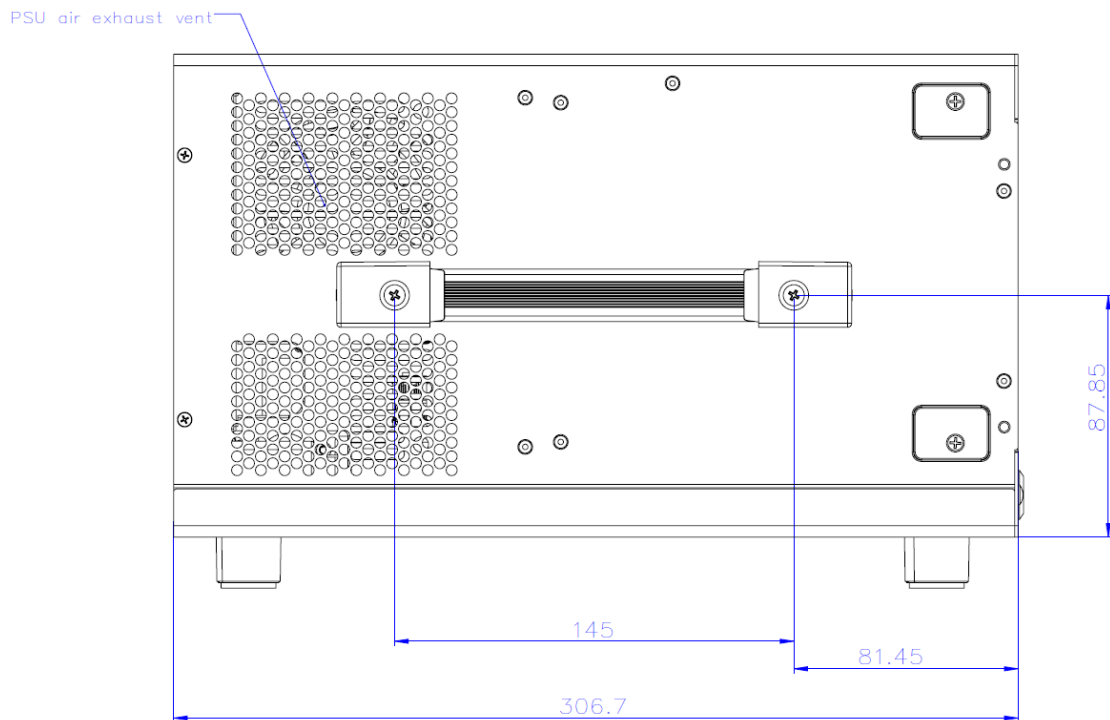


Figure 4 Left Side View (PXle-2518G3/G2)

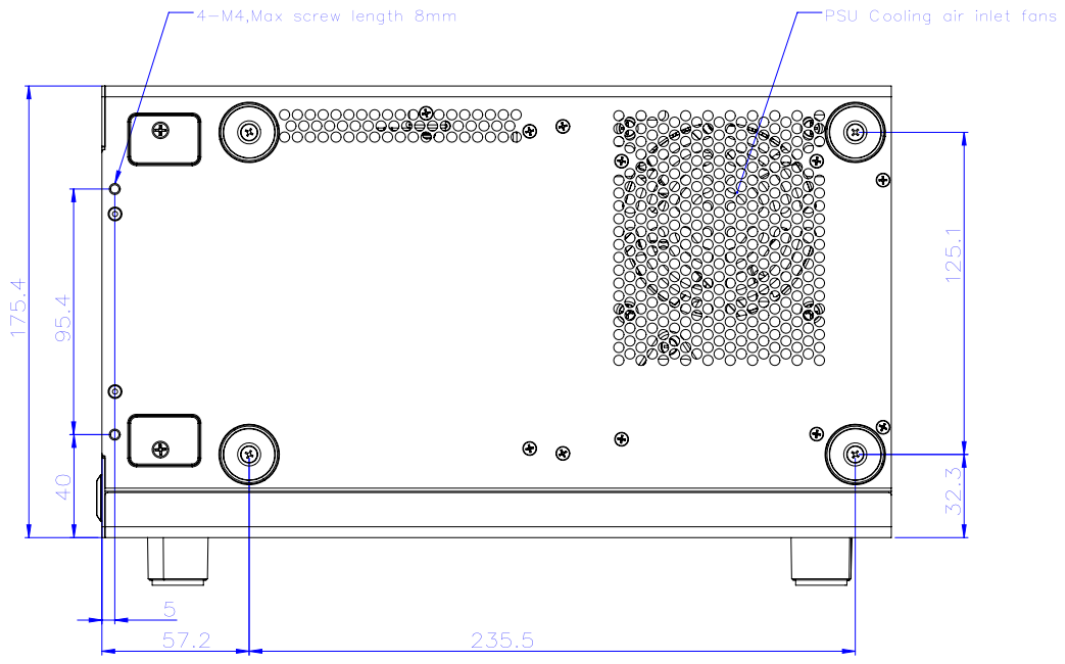


Figure 5 Right Side View (PXle-2518G3/G2)

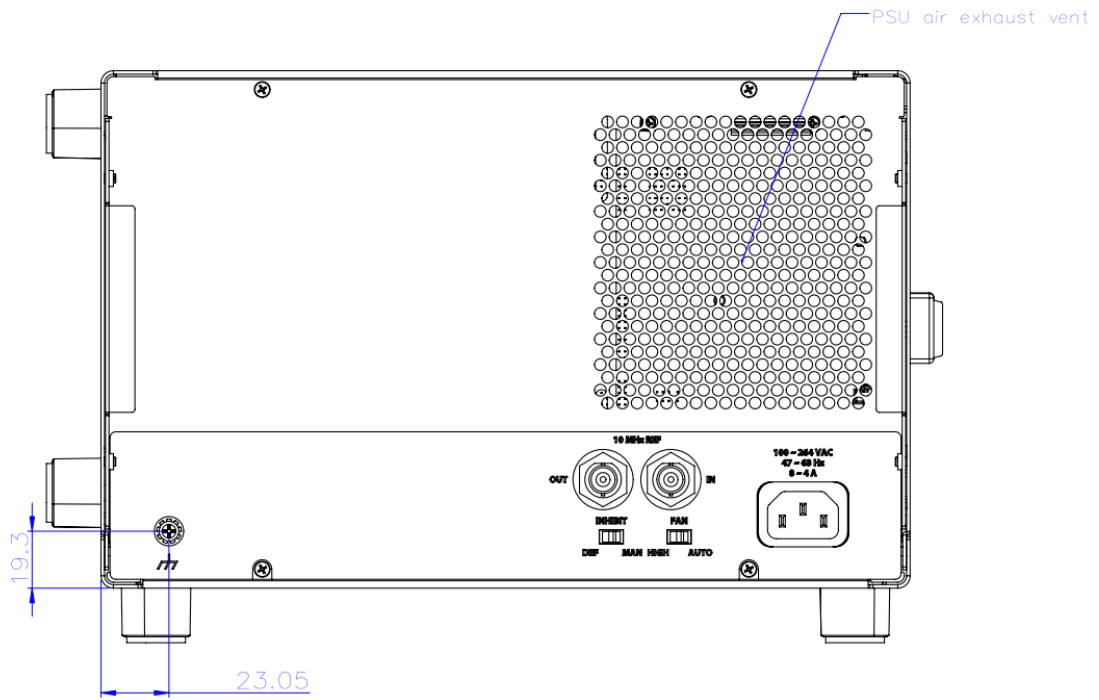


Figure 6 Rear View (PXle-2518G3/G2)

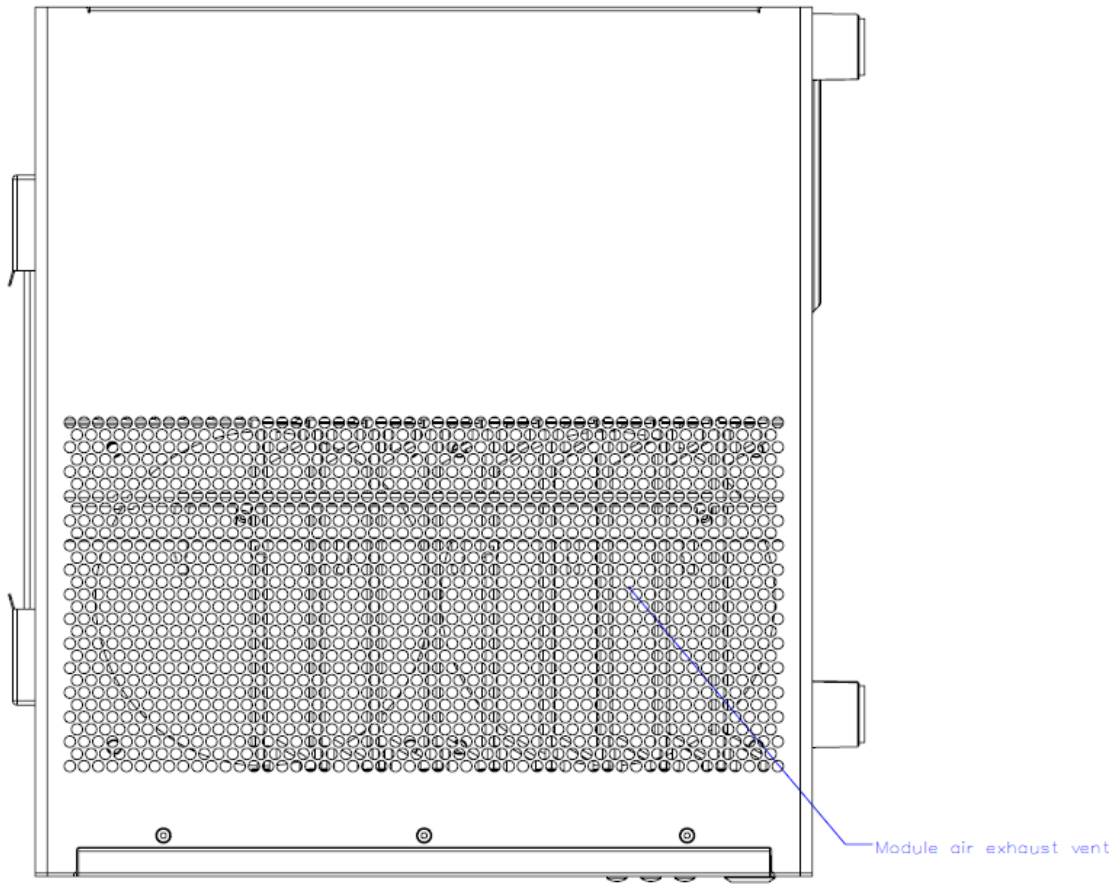


Figure 7 Top View (PXIe-2518G3/G2)



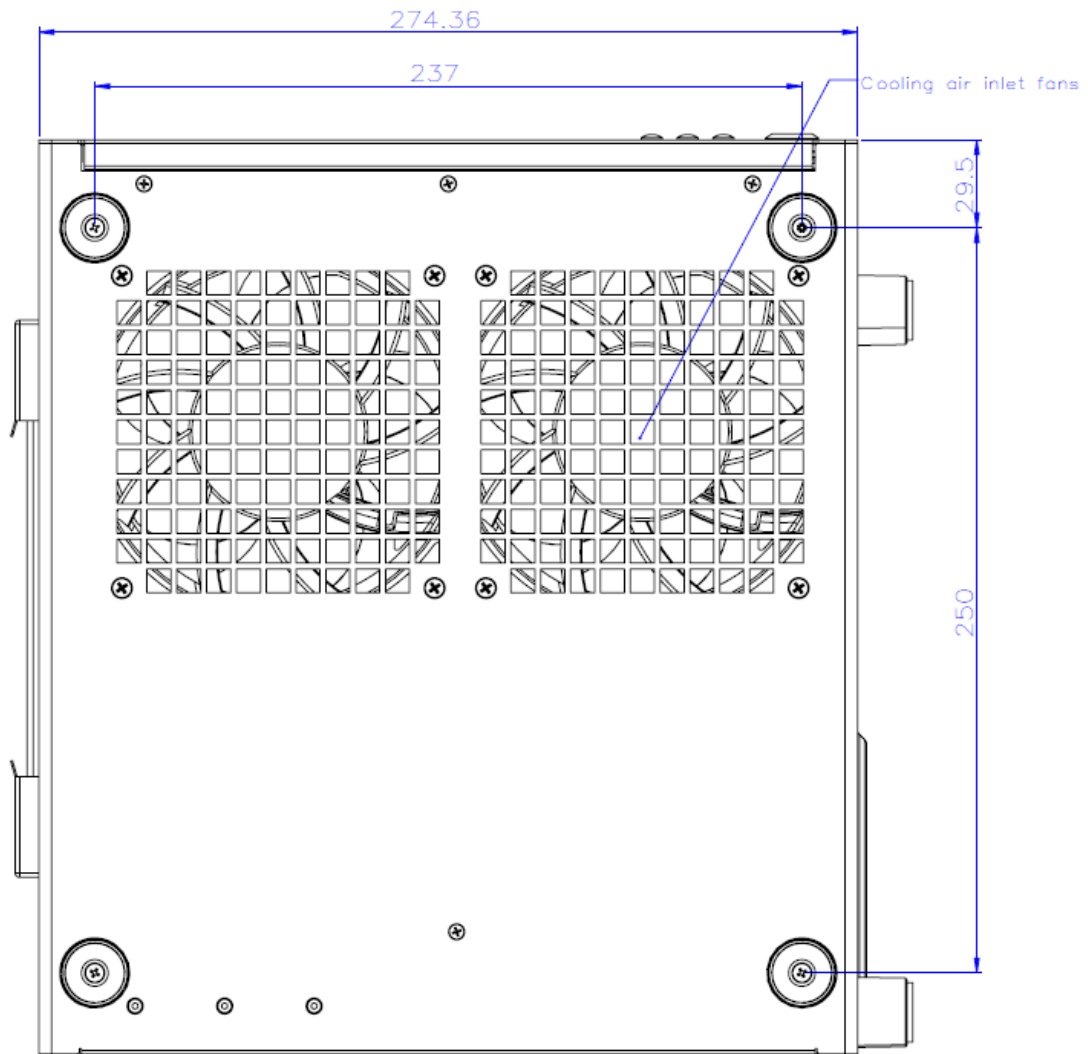


Figure 8 Bottom View (PXIe-2518G3/G2)

## 2.4 Front and Rear Panels

### 2.4.1 Front Panel

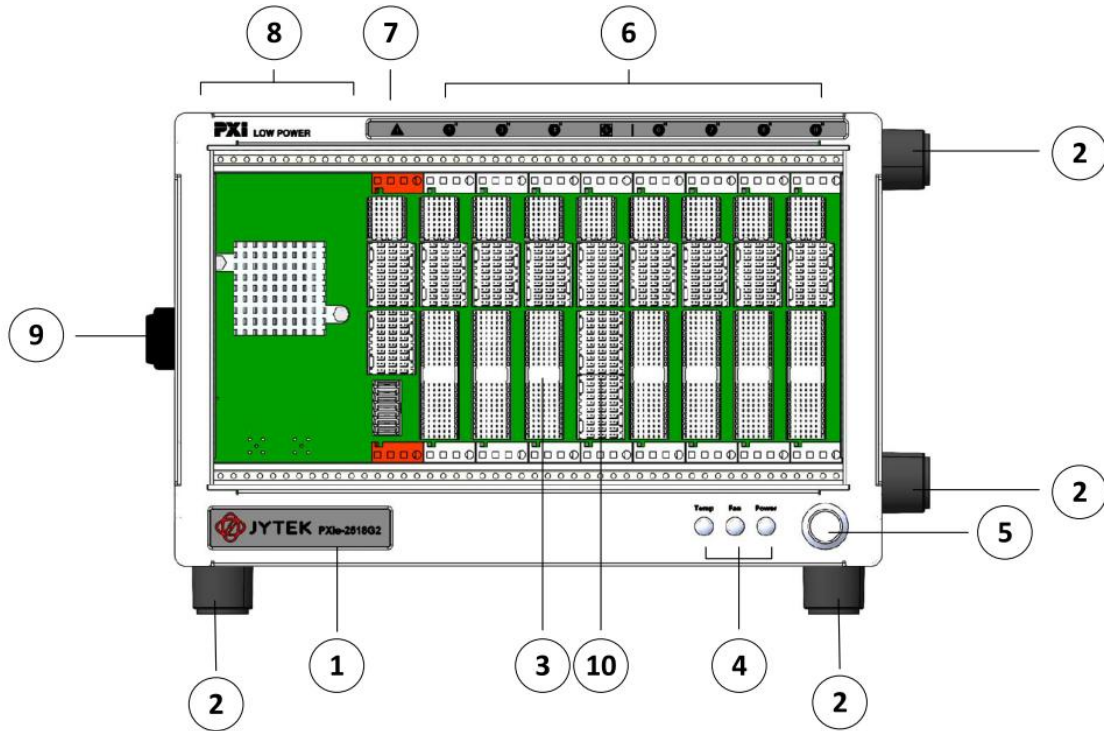


Figure 9 Front Panel

	Feature
1	Chassis Model Name
2	Removable Feet
3	Backplane Connectors
4	Chassis Status LED
5	Power Switch
6	PXI Express Hybrid Peripheral Slots
7	PXI Express System Controller Slot
8	System Controller Expansion Slots
9	Handle
10	System Timing Slot

Table 8 Front Panel

### 2.4.2 Rear Panel

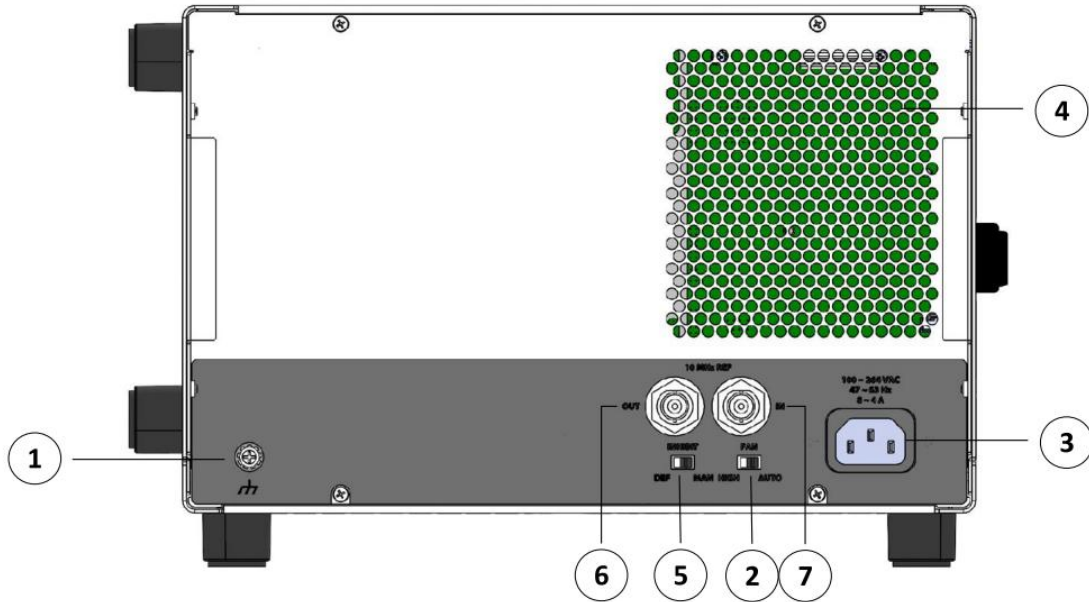


Figure 10 PXIe-2518G2/G3 Rear Panel

	Feature
1	Chassis Ground Screw
2	FAN Switch
3	AC Input
4	Rear Output Vents
5	Inhibit Switch
6	10M Clock Output
7	10M Clock Input

Table 9 PXIe-2518G2/G3 Rear Panel

### 2.4.3 Chassis Status LED

Chassis Status LED	Temp LED (Amber)	Fan LED (Green)	Power LED (Blue)
On	Chassis MCU is abnormal	Fan is normal	Power is normal
Off	Temperature is normal	Chassis is powered down	Chassis is powered down
Blinking	Temperature sensors exceeds threshold temperature (default is 70°C)	Fan falls below threshold speed (default is 800RPM)	Power rail exceeds threshold setting (default is ±5% )

Table 3 Chassis Status LED

### 2.4.4 Fan Mode

PXle-2518 provides the smart fan control mechanism as blow curve. It provides two fan modes.

Fan Mode	Fan's duty cycle	Fan's speed	Note
<b>AUTO</b>	40% ~ 100%	1100 rpm ±10%	Based on temperature
<b>HIGH</b>	100%	4300 rpm ±10%	

Table 4 Fan Mode

When the **Fan Switch** is set to **AUTO** mode, the fan speed is controlled based on the measured temperature of sensor.

Fans run at 40% duty cycle if the measured temperature less than 40°C, and begin ramping up when any temperature reading exceeds 40°C.

Fans run at 100% duty cycle (full speed) if any temperature reading exceeds 65°C.

When the **Fan Switch** is set to **HIGH** mode, fans run at 100% duty cycle immediately.

The factory default fan control curve shows as following Figure.

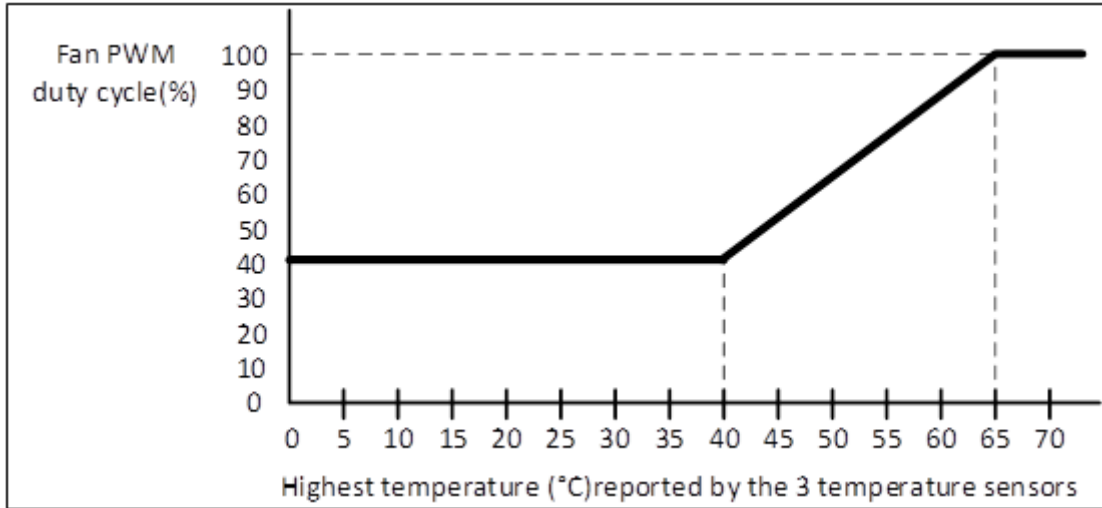


Figure 8 Fan Control Curve

## 2.5 Chassis Cooling Considerations

### 2.5.1 PXI/PXIe Modules Cooling

For PXI/PXIe modules cooling, there are two fans on the underside of the chassis draw cool air from the bottom side of chassis to be exhausted to the top side of the chassis.

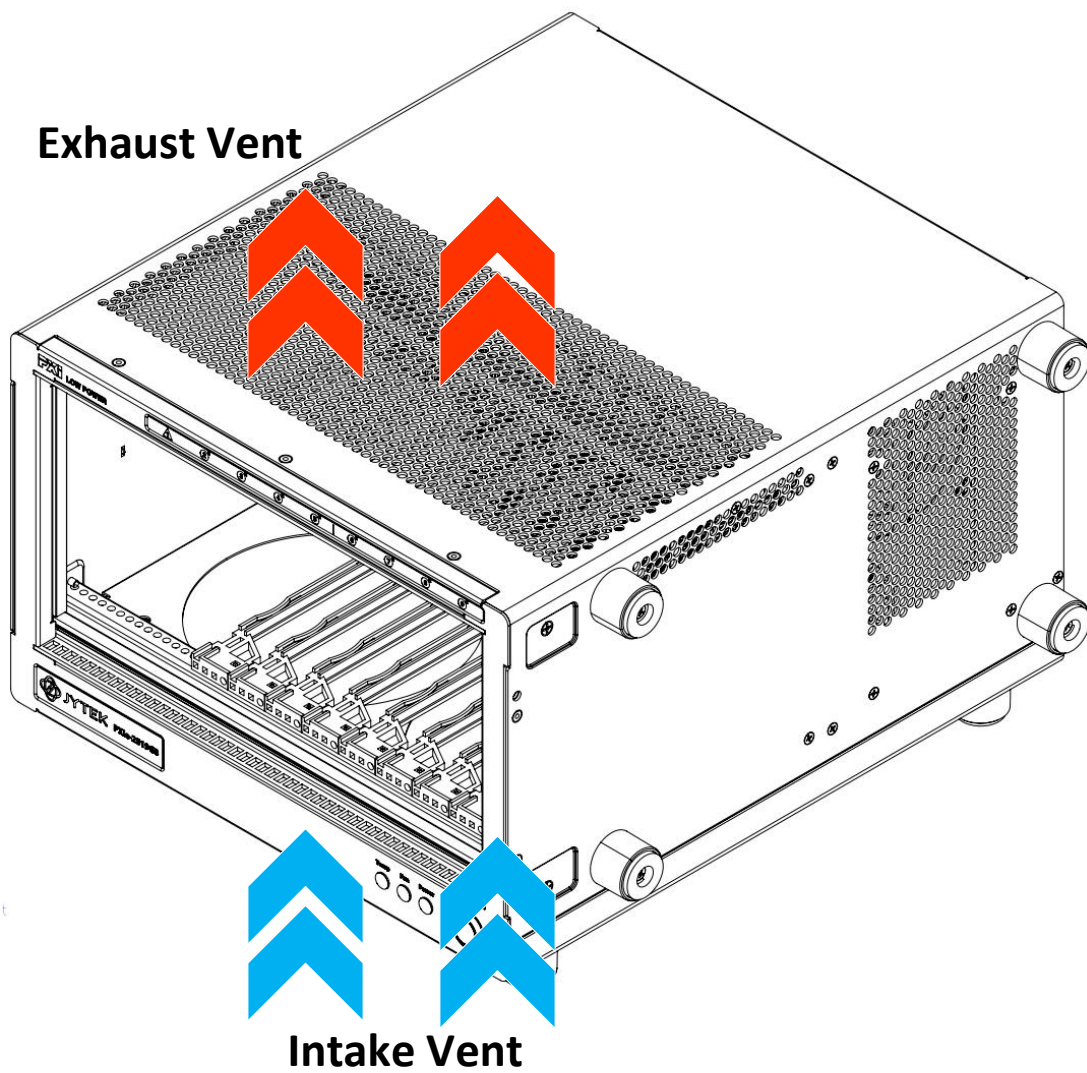


Figure 9 PXI/PXIe Modules Cooling

### 2.5.2 Power Supply Cooling

For power supply cooling, power supply's fan draws cool air from the right side, to be exhausted through the left side and rear side of the chassis.

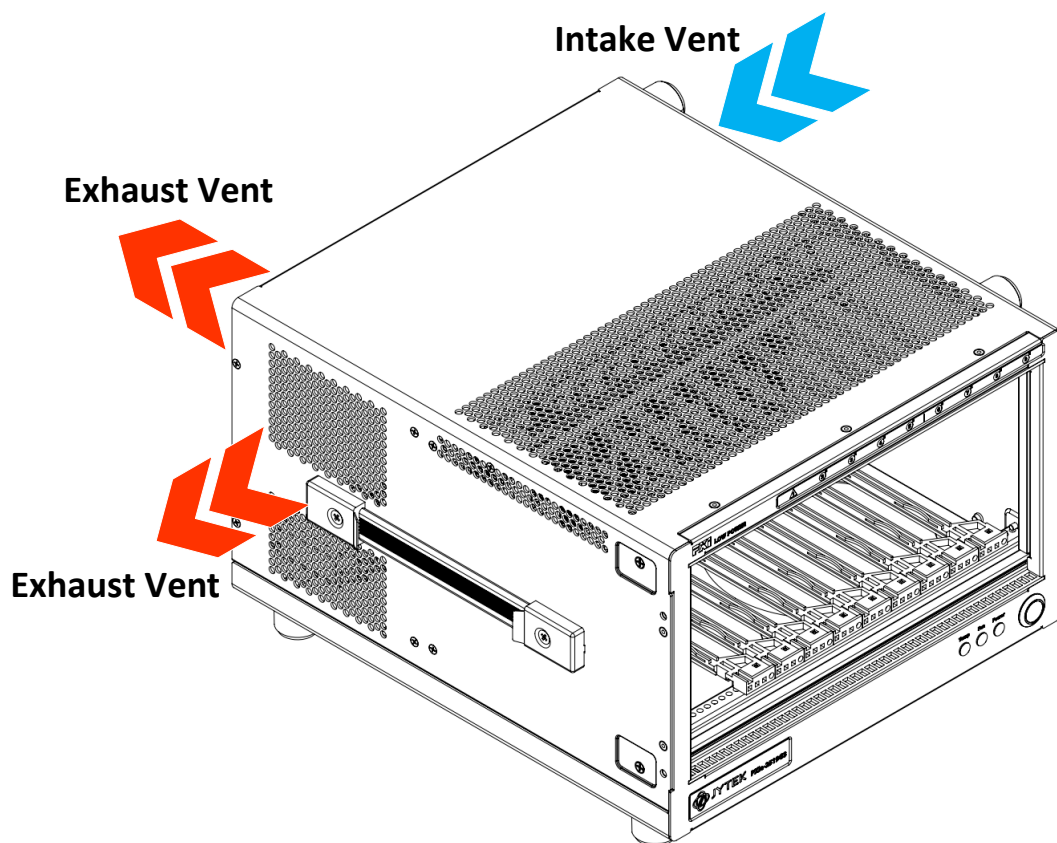
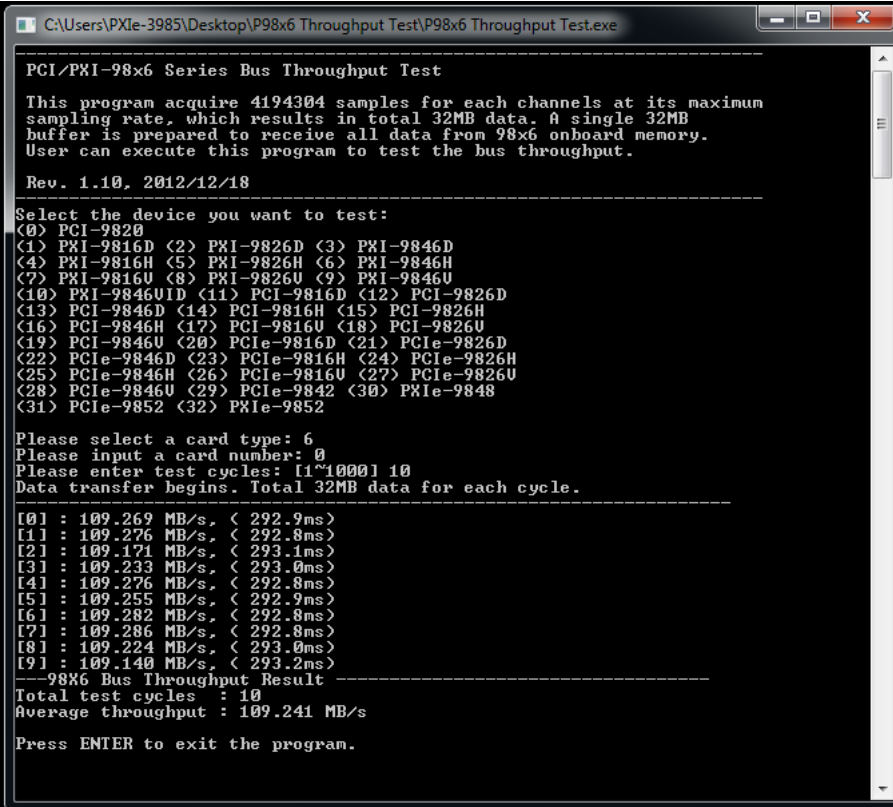


Figure 10 Power Supply Cooling

### 3. Performance Test

#### 3.1 PCI Bus Throughput

PXIe-2518G3/G2/DC provides excellent throughput of PCI Bus as shown in below. There are two PCI Bus segments in the backplane. Slot2 to Slot4 is segment 1, and Slot6 to Slot9 is segment 2.



```
C:\Users\PXIe-3985\Desktop\P98x6 Throughput Test\P98x6 Throughput Test.exe
PCI/PXI-98x6 Series Bus Throughput Test
This program acquire 4194304 samples for each channels at its maximum
sampling rate, which results in total 32MB data. A single 32MB
buffer is prepared to receive all data from 98x6 onboard memory.
User can execute this program to test the bus throughput.
Rev. 1.10, 2012/12/18
-----
Select the device you want to test:
<0> PCI-9820
<1> PXI-9816D <2> PXI-9826D <3> PXI-9846D
<4> PXI-9816H <5> PXI-9826H <6> PXI-9846H
<7> PXI-9816U <8> PXI-9826U <9> PXI-9846U
<10> PXI-9846UID <11> PCI-9816D <12> PCI-9826D
<13> PCI-9846D <14> PCI-9816H <15> PCI-9826H
<16> PCI-9846H <17> PCI-9816U <18> PCI-9826U
<19> PCI-9846U <20> PCIe-9816D <21> PCIe-9826D
<22> PCIe-9846D <23> PCIe-9816H <24> PCIe-9826H
<25> PCIe-9846H <26> PCIe-9816U <27> PCIe-9826U
<28> PCIe-9846U <29> PCIe-9842 <30> PXIe-9848
<31> PCIe-9852 <32> PXIe-9852
Please select a card type: 6
Please input a card number: 0
Please enter test cycles: [1~1000] 10
Data transfer begins. Total 32MB data for each cycle.
-----
[0] : 109.269 MB/s, < 292.9ms>
[1] : 109.276 MB/s, < 292.8ms>
[2] : 109.171 MB/s, < 293.1ms>
[3] : 109.233 MB/s, < 293.0ms>
[4] : 109.276 MB/s, < 292.8ms>
[5] : 109.255 MB/s, < 292.9ms>
[6] : 109.282 MB/s, < 292.8ms>
[7] : 109.286 MB/s, < 292.8ms>
[8] : 109.224 MB/s, < 293.0ms>
[9] : 109.140 MB/s, < 293.2ms>
-----98x6 Bus Throughput Result -----
Total test cycles : 10
Average throughput : 109.241 MB/s
Press ENTER to exit the program.
```

Figure 11 PCI Bus Throughput for segment 1



```

C:\Users\PXIe-3985\Desktop\P98x6 Throughput Test\P98x6 Throughput Test.exe
-----
PCI/PXI-98x6 Series Bus Throughput Test

This program acquire 4194304 samples for each channels at its maximum
sampling rate, which results in total 32MB data. A single 32MB
buffer is prepared to receive all data from 98x6 onboard memory.
User can execute this program to test the bus throughput.

Rev. 1.10, 2012/12/18
-----
Select the device you want to test:
<0> PCI-9820
<1> PXI-9816D <2> PXI-9826D <3> PXI-9846D
<4> PXI-9816H <5> PXI-9826H <6> PXI-9846H
<7> PXI-9816U <8> PXI-9826U <9> PXI-9846U
<10> PXI-9846UID <11> PCI-9816D <12> PCI-9826D
<13> PCI-9846D <14> PCI-9816H <15> PCI-9826H
<16> PCI-9846H <17> PCI-9816U <18> PCI-9826U
<19> PCI-9846U <20> PCIe-9816D <21> PCIe-9826D
<22> PCIe-9846D <23> PCIe-9816H <24> PCIe-9826H
<25> PCIe-9846H <26> PCIe-9816U <27> PCIe-9826U
<28> PCIe-9846U <29> PCIe-9842 <30> PXIe-9848
<31> PCIe-9852 <32> PXIe-9852

Please select a card type: 6
Please input a card number: 0
Please enter test cycles: [1~1000] 10
Data transfer begins. Total 32MB data for each cycle.
-----
[0] : 109.274 MB/s, < 292.8ms>
[1] : 109.279 MB/s, < 292.8ms>
[2] : 109.177 MB/s, < 293.1ms>
[3] : 109.249 MB/s, < 292.9ms>
[4] : 109.258 MB/s, < 292.9ms>
[5] : 109.259 MB/s, < 292.9ms>
[6] : 109.272 MB/s, < 292.8ms>
[7] : 109.251 MB/s, < 292.9ms>
[8] : 109.278 MB/s, < 292.8ms>
[9] : 109.278 MB/s, < 292.8ms>
-----98x6 Bus Throughput Result -----
Total test cycles : 10
Average throughput : 109.258 MB/s

Press ENTER to exit the program.
-

```

Figure 13 PCI Bus Throughput for segment 2

PCI Bus Segment	Slot	Test Module	Test Result
Segment 1	2	PXI-69846H	109 MB/s
	3	PXI-69846H	109 MB/s
	4	PXI-69846H	109 MB/s
Segment 2	6	PXI-69846H	109 MB/s
	7	PXI-69846H	109 MB/s
	8	PXI-69846H	109 MB/s
	9	PXI-69846H	109 MB/s

Table 10 PCI Bus Throughput

Note:

- PCI Bus theoretical maximum bandwidth is 132 MB/s.
- PXI-69846H is 4-ch 40 MS/s 16-bit digitizer, its bandwidth is 320 MB/s.

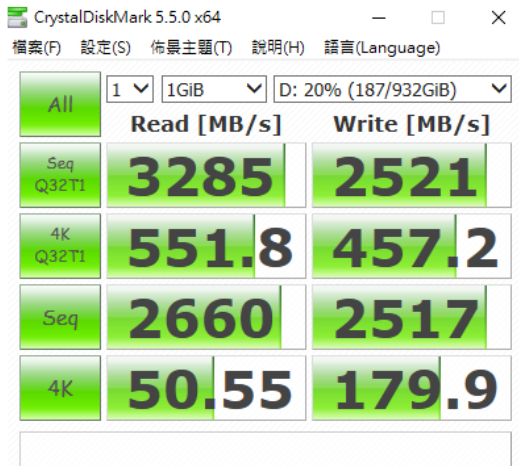
### 3.2 PCIe Bus Throughput

PXle-2518G3 provides excellent throughput of PCIe Bus as shown in below.

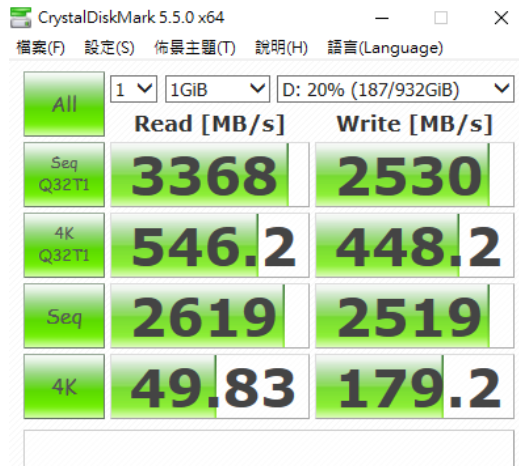
Slot	Fixture	Test Result
2	PXle-63987 + PXle-825 + Samsung 970 EVO SSD 1TB	Upstream: 3.2GB/s Downstream: 2.5GB/s
3	PXle-63987 + PXle-825 + Samsung 970 EVO SSD 1TB	Upstream: 3.3GB/s Downstream: 2.5GB/s
4	PXle-63987 + PXle-825 + Samsung 970 EVO SSD 1TB	Upstream: 3.2GB/s Downstream: 2.5GB/s
5	PXle-63987 + PXle-825 + Samsung 970 EVO SSD 1TB	Upstream: 3.3GB/s Downstream: 2.5GB/s

Table 11 PCIe Bus Throughput

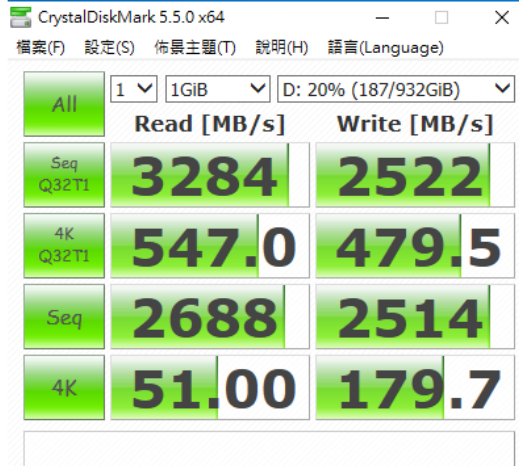
#### Slot2:



#### Slot3:



#### Slot4:



#### Slot5:

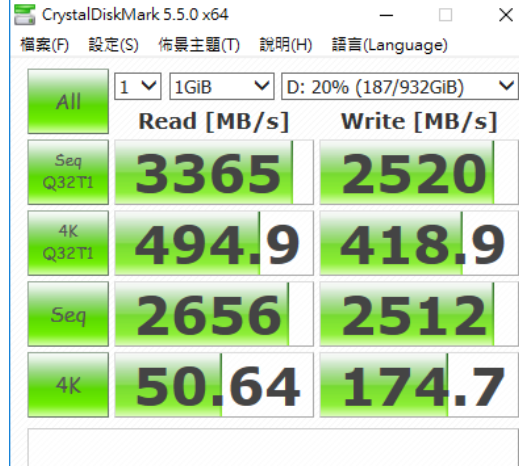


Figure 12 PCIe Bus Throughput

Note:

- Slot 1 is the system bandwidth test; its theoretical maximum bandwidth is 16 GB/s (PCIe Gen3 x16).
- Slot 2 to 5 are the slot bandwidth test; its theoretical maximum bandwidth is 4 GB/s (PCIe Gen3 x4).

## 4. Software

### 4.1 Introduction to JYDM

**JYDM (JYTEK Device Management)** is the latest equipment management software of JYTEK. Its main functions are as follows:

- Support GUI information display and management of PXI-2/6 standard equipment.
- Support trigger configuration of PXI-9 standard chassis.
- JYTEK self-developed chassis information management.
- JYTEK self-developed card: alias management, driver and firmware online upgrade, online driver version management, board test panel.
- JYTEK SeeSharp card: driver information view, test panel.

### 4.2 Installation and use of JYDM

**JYDM** support operating system: Windows 7 32/64 bit, Windows 10 32/64 bit.

1. Install **.Net framework** (version 4.0 or above).
2. Download and install **FirmDrive** (version 1.3.3 or above) from the official website of JYTEK.
3. Download and Install the JYTEK **peripheral module driver** from the official website of JYTEK.
4. Download and install the **JYDM** installation package from the official website of JYTEK.



Figure 13 Install the JYDM

After the software installation complete, open JYDM and you will see the chassis, controller and peripheral module in the overall system as shown in the figure below.

Note:

- JYDM usually requires a few seconds to scan device.

The left side of the JYDM interface is the hardware device column, and the right side is the device details column. You can view and configure the current device information, and upgrade the driver and firmware.

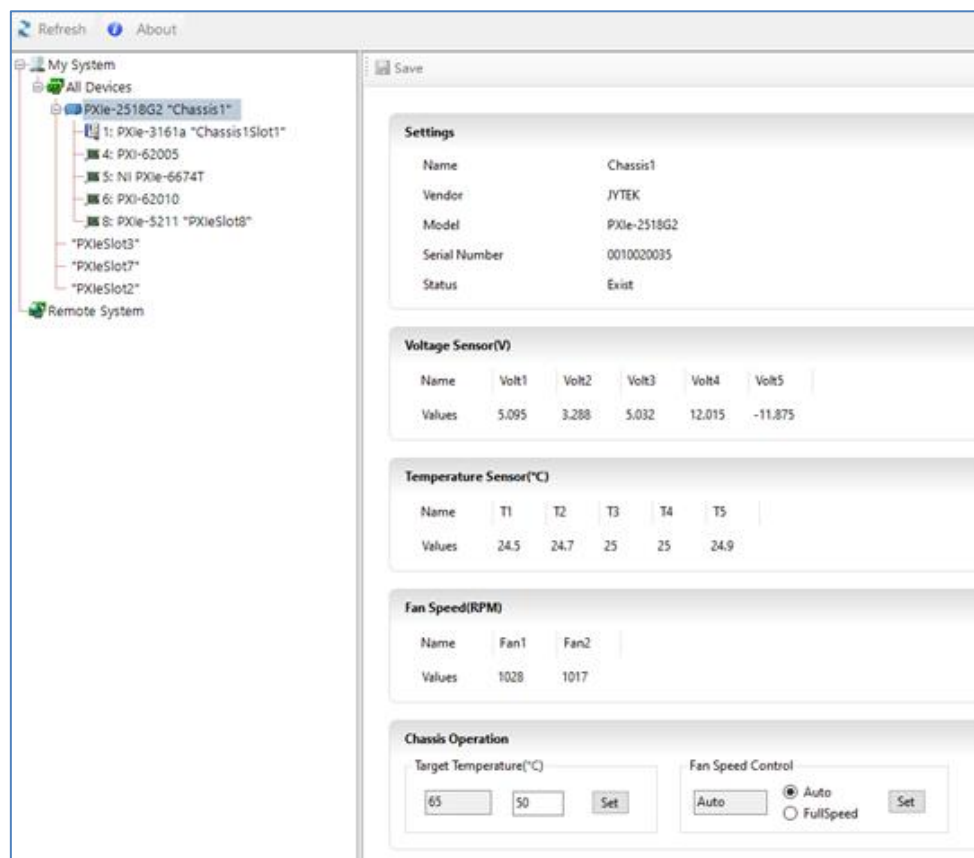


Figure 15 JYDM GUI application program

Note:

- JYTEK peripheral module driver has two parts: the shared common driver kernel software (FirmDrive) and the specific peripheral module driver.
- After firmware update of peripheral module, you need to **cold restart** your device.
- After driver update of peripheral module, you need to **warm restart** your device.

### 4.3 Chassis environment monitoring in JYDM

The JYDM provides the following chassis environment monitoring capabilities:

- Monitoring the chassis power rails: 5Vsb (standby power), 3.3V, 5V, 12V and -12V DC power.

Voltage Sensor(V)					
Name	Volt1	Volt2	Volt3	Volt4	Volt5
Values	5.084	3.28	5.073	12.044	-11.964

Figure 14 Monitoring the Chassis Power Rails

- Monitoring the chassis temperature sensors.  
(T1 sensor is located on the top side of slot1.)

Temperature Sensor(°C)					
Name	T1	T2	T3	T4	T5
Values	25.3	25.1	24.8	24.8	24.8

Figure 15 Monitoring the Chassis Temperature Sensors

- Monitoring the chassis fan speed.  
(Fan1 module is located on the bottom side of slot1.)

Fan Speed(RPM)		
Name	Fan1	Fan2
Values	1139	1128

Figure 16 Monitoring the Chassis Fan Speed

## 4.4 Chassis cooling control in JYDM

PXIe-2518 chassis allow user to control the cooling capability via JYDM.

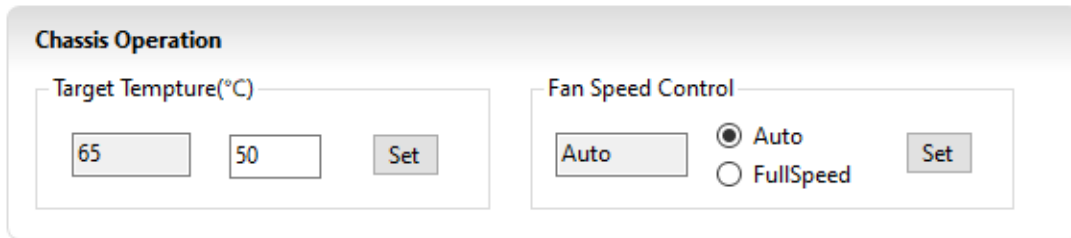


Figure 17 Chassis Cooling Control in JYDM

**Target Temperature** specifies the chassis temperature at which the maximum fan speed (100% duty cycle) is achieved as shown in below figure.

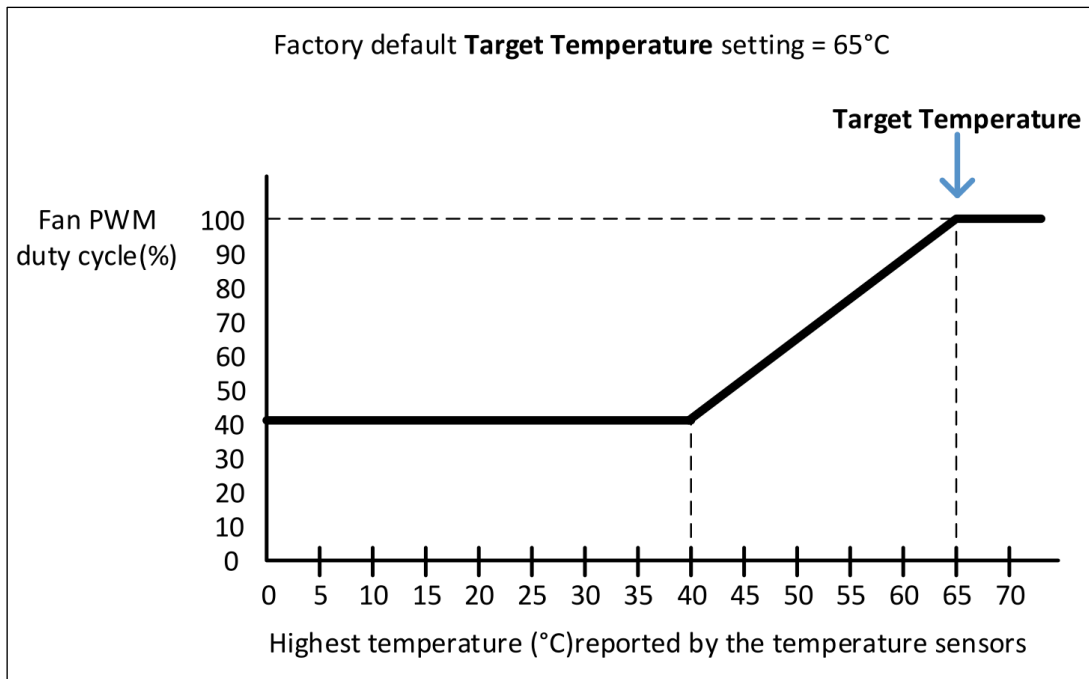


Figure 16 Factory default Target Temperature setting

The factory default target temperature setting is 65 °C. User can change target temperature to lower value (ex. 45 °C), it will increase fan speed if the factory default setting could not fulfill the peripheral modules cooling requirement.

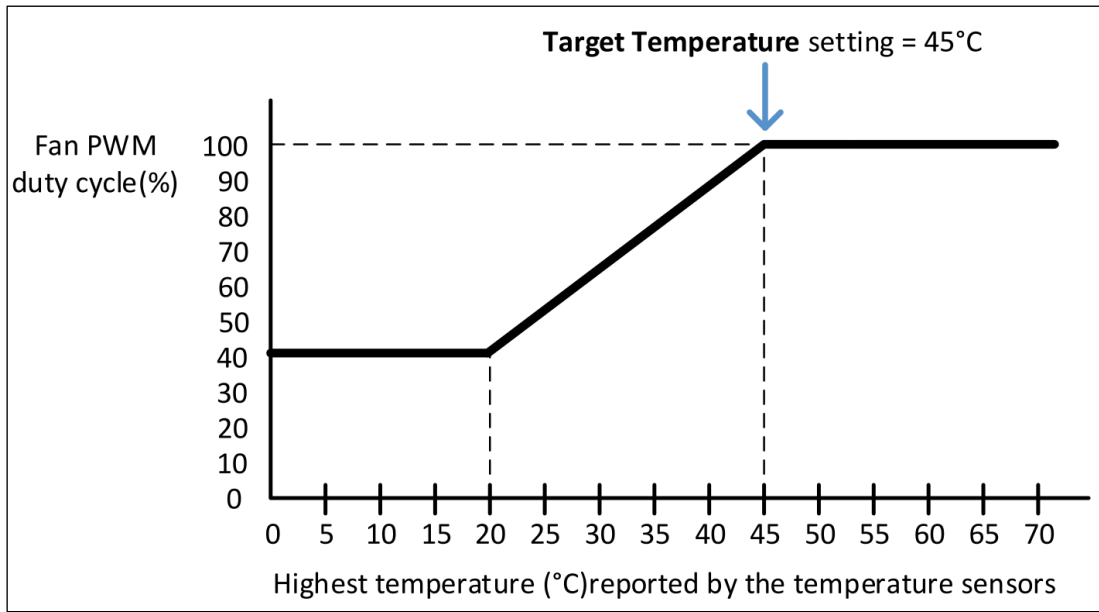


Figure 17 Change Target Temperature to 45 °C



## 4.5 Reference Clock Status Display in JYDM

JYDM can display the 10MHz reference clock(PXI\_CLK10) source which come from onboard (backplane's local oscillator) or external (rear panel's BNC connector). The default clock source is **On Board** as shown in figure 18.



Figure 18 Reference Clock Status Display for default setting

If the external 10MHz clock input the chassis via BNC connector, or 10MHz clock from system timing slot, it will override the onboard 10MHz clock. A phase-lock loop (PLL) circuit on the backplane synchronizes the PXIe\_CLK100 and external 10MHz clock, and then JYDM will display **Synchronized** and green indicator as shown in figure 19.



Figure 18 Reference Clock Status Display for external clock source

## 4.6 Chassis identification in NI MAX

Download and install NI PXI platform services 20.0 or higher from NI website:



Figure 20 Install NI MAX

Open **JYDM**, set **Valid PXI Resource Manager** and **Default PXI Trigger Manger** to National Instruments, and then click **Save** to save the settings.

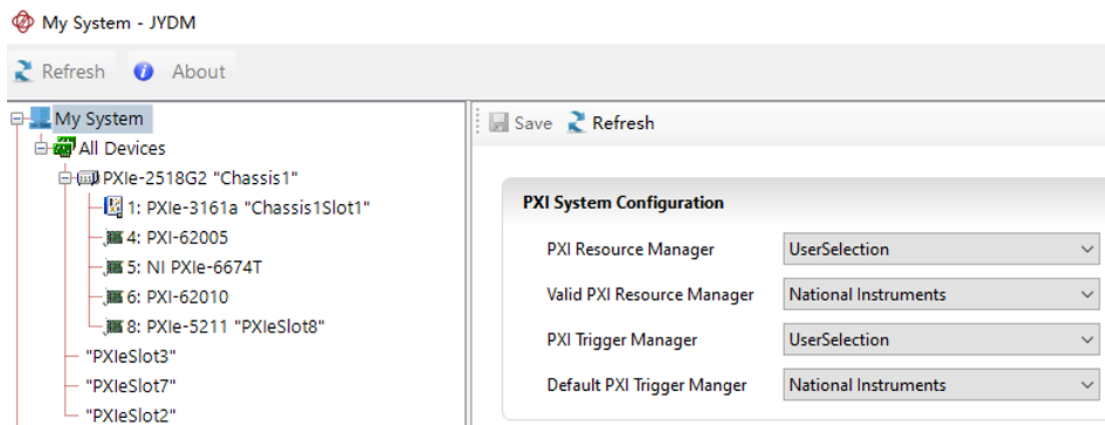


Figure 21 Change PXI Trigger Manager Setting

Open NI MAX after software installation and the devices can be identified:

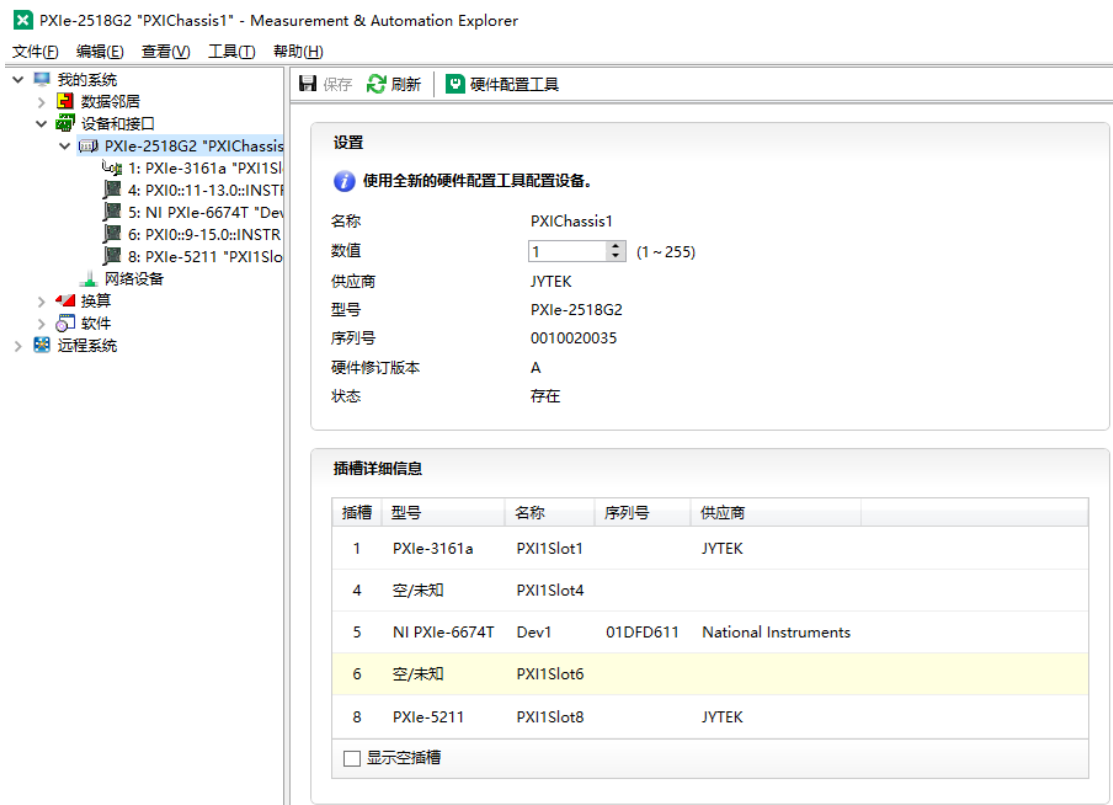


Figure 22 NI MAX GUI display JYTEK chassis and modules

## 5. Using PXIe-2518 Chassis

This chapter provides the operation guides for PXIe-2518.

### 5.1 Using PXIe-2518 with JYTEK PXI/PXIe Peripheral Modules

Using PXIe-2518 with JYTEK PXI/PXIe peripheral modules is straightforward. JYTEK also provide a device management software to view the modules in the chassis. For more information, please visit our web [www.jytek.com](http://www.jytek.com) to download.

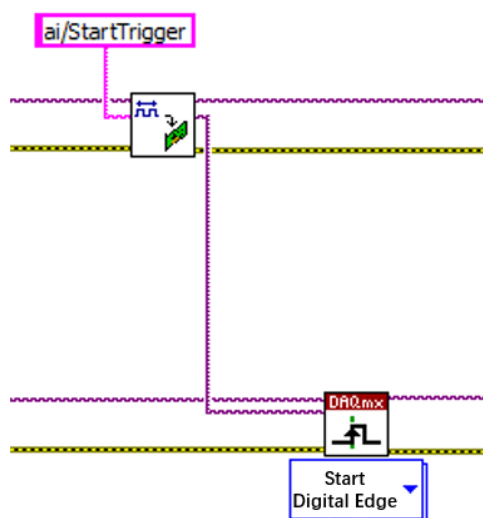
### 5.2 Using PXIe-2518 with National Instruments PXI/PXIe Peripheral Modules

#### 5.2.1 Use National Instruments PXI/PXIe Peripheral Modules without synchronization:

You can use the modules as usual without any additional setting.

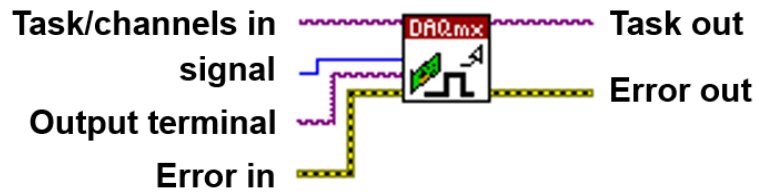
#### 5.2.2 Use National Instruments PXI/PXIe Peripheral Modules with synchronization:

A few vi like "Get Full Terminal Name.vi" cannot use on the third party chassis:



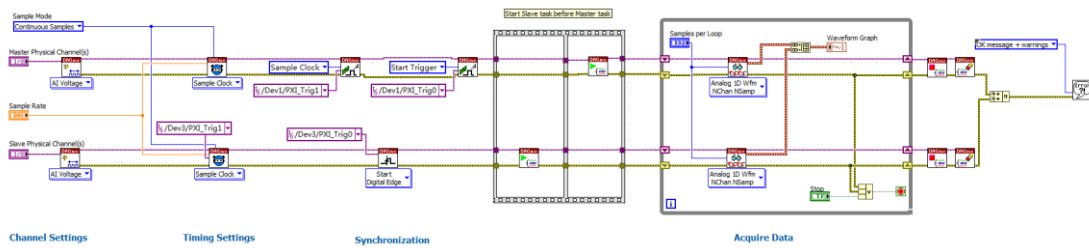
But you can use "DAQmx Export Signal" to set appointed clock/trigger routing:

## DAQmx Export Signal (Most Signals).VI



Routes a control signal to the terminal you specify. The output terminal can reside on the device that generates the control signal or on a different device. You can use this VI to share clocks and triggers among multiple tasks and devices. The routes this VI creates are task-based routes.

DAQ synchronization reference code:



## 6. Optional Equipment

### 6.1 Rack Mount Kits

JYTEK provides optional hardware for installation of PXIe-2518 chassis into a server or rack. The rack mounting kits dimension as following figure. All dimensions are shown in mm (millimeters).

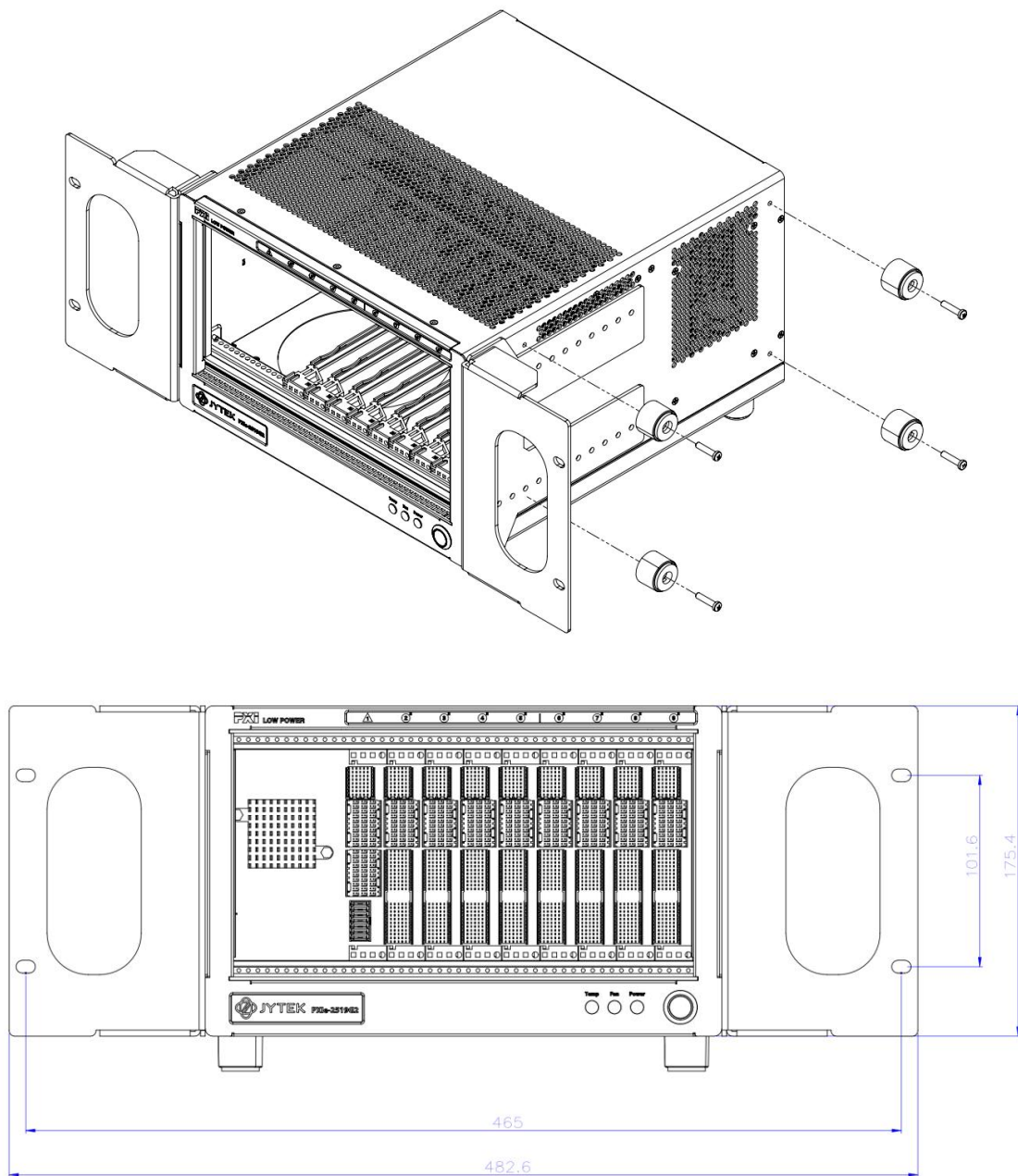


Figure 23 PXIe-2518 rack mount kits dimension

## **7. About JYTEK**

### **7.1 JYTEK China**

Founded in June, 2016, JYTEK China is a leading Chinese test & measurement company, providing complete software and hardware products for the test and measurement industry. The company is a joint venture between Adlink Technologies and a group of experienced professionals from the industry. JYTEK independently develop the software and hardware products and is entirely focused on the Chinese market. Our Shanghai headquarters and production service center have regular stocks to ensure timely supply; we have R&D centers in Xi'an and Chongqing to develop new products; we also have highly trained direct technical sales representatives in Shanghai, Beijing, Tianjin, Xi'an, Chengdu, Nanjing, Wuhan, Haerbin, and Changchun. We also have many partners who provide system level support in various cities.

### **7.2 JYTEK Hardware Products**

According to JYTEK's agreement with our equity partner Adlink Technologies, JYTEK's hardware is manufactured by the state-of-art manufacturing facility located in Shanghai Zhangjiang Hi-Tech Park. Adlink has over 20 years of the world-class low-volume and high-mix manufacturing expertise with ISO9001-2008, China 3C, UL, ROHS, TL9000, ISO-14001, ISO-13485 certifications. Its 30,000 square meters facilities and three high-speed Panasonic SMT production lines can produce 60,000 pieces boards/month; it also has full supply chain management - planning, sweeping, purchasing, warehousing and distribution. Adlink's manufacturing excellence ensures JYTEK's hardware has world-class manufacturing quality.

One core technical advantage is JYTEK's pursue for the basic and fundamental technology excellence. JYTEK China has developed a unique PCIe, PXIe, USB hardware driver architecture, FirmDrive, upon which many our future hardware will be based.

In addition to our own developed hardware, JYTEK also rebrands Adlink's PXI product lines. In addition, JYTEK has other rebranding agreements to increase our hardware

coverage. It is our goal to provide the complete product coverage in PXI and PCI modular instrumentation and data acquisition.

### **7.3 JYTEK Software Platform**

JYTEK has developed a complete software platform, SeeSharp Platform, for the test and measurement applications. We leverage the open sources communities to provide the software tools. Our platform software is also open sourced and is free, thus lowering the cost of tests for our customers. We are the only domestic vendor to offer complete commercial software and hardware tools.

### **7.4 JYTEK Warranty and Support Services**

With our complete software and hardware products, JYTEK is able to provide technical and sales services to wide range of applications and customers. In most cases, our products are backed by a 1-year warranty. For technical consultation, pre-sale and after-sales support, please contact JYTEK of your country.



## **8. Statement**

The hardware and software products described in this manual are provided by JYTEK China, or JYTEK in short.

This manual provides the product review, quick start, some explanation for JYTEK PXIe-2518 chassis. The manual is copyrighted by JYTEK.

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While we try to keep this manual up to date, there are factors beyond our control that may affect the accuracy of the manual. Please check the latest manual and product information from our website.

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